

1. Schematic Page Description :

Origins Schematic Ver :

01

SoC I2C table

Function	Channel	Read	Write
Touch Screen	I2C0	0x?	
Audio Codec	I2C1	0x?	0x?
VNN (reserve)	I2C4		
Track Pad	I2C5		
EC	I2C6		

EC SMBus/I2C table

Function	Channel	Address
Battery/Thermal	SMB0	
NA	SMB1	
G-Sensor	I2C1	
PCH	I2C2	
VNN	I2C3	

Current sensor address

Function	Channel	Function	Channel
+VBATA	0x47	+VCC_OUT	0x40
+V5A	0x43	+VGG	0x44
+V3P3A	0x4B	+VNN	0x45
+V1P05A	0x46	+VDDQ_OUT	0x41
+V1P8A	0x49		

USB3/2 port mapping

USB3 Port No#	Usage	USB2 Port No#	Usage
USB3P0	NA	USB2P0	I/O(2.0)
USB3P1	NA	USB2P1	LTE
USB3P2	I/O	USB2P2	I/O(3.0)
USB3P3	NA	USB2P3	CCD
		USB2P4	BT

PCIe port mapping

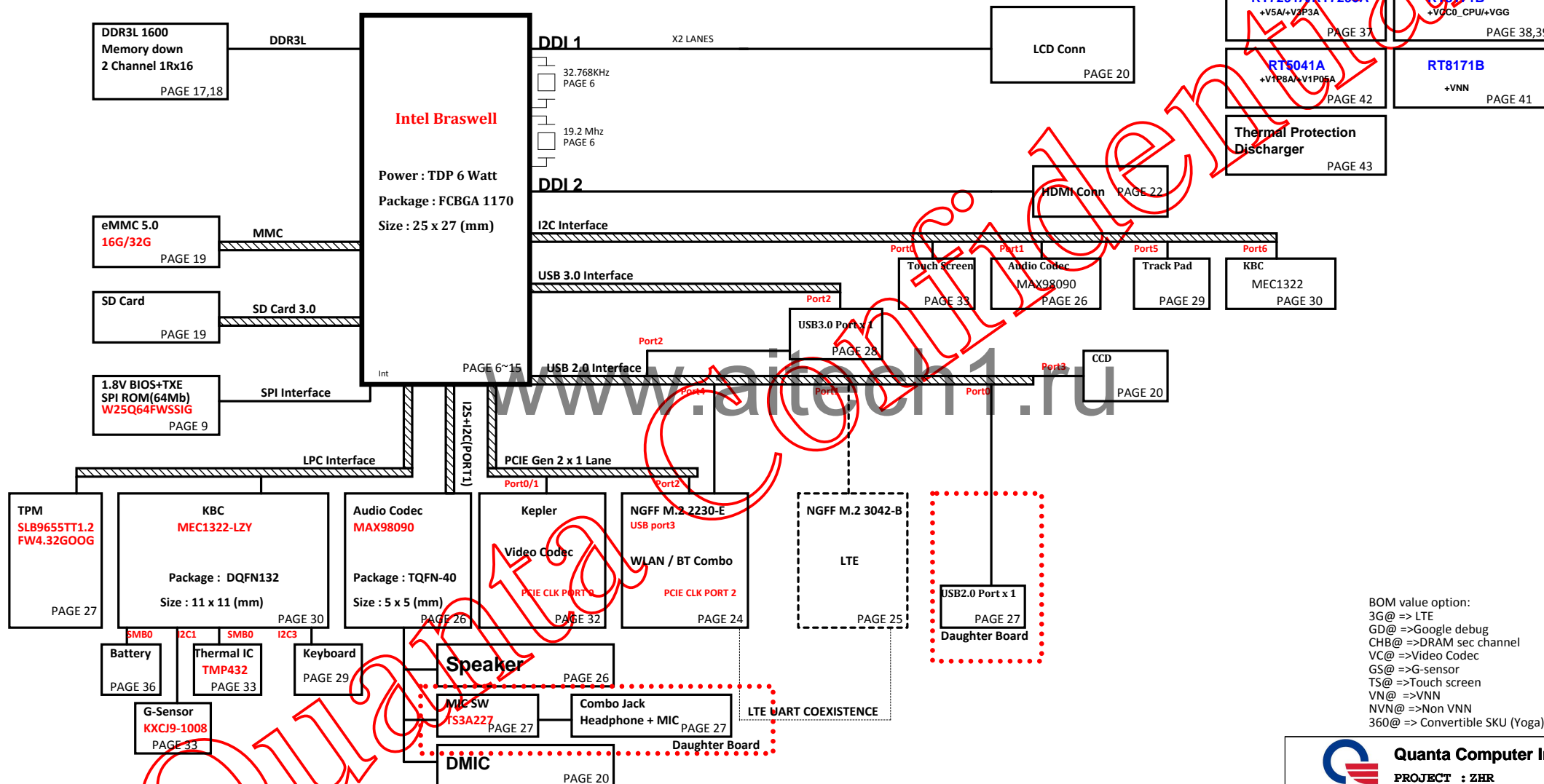
PCIe port No#	Usage	PCIe CLK#	Usage
PCIe_0	Video Codec	PCIe_CLK0	Video Codec
PCIe_1	Video Codec	PCIe_CLK1	NA
PCIe_2	WLAN	PCIe_CLK2	WLAN
PCIe_3	NA	PCIe_CLK3	NA

Intel Braswell Platform Block Diagram

For ZHRA_DVT SKU1 AJ0QJ4VVT04--CPU(1170)BSWN3050 1.6G QJ4V(FCBGA)STNBSQ

For ZHRA_SKU2/3 AJ0QJ4TVT03--CPU(1170)BSWN3150 1.6G QJ4T(FCBGA)STNBSQ

Default BOM is SKU2



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	BSW 1/10 (DDRA)	1A
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BSW_MCP_EDS
REV = 1

Size	Document Number BSW 2/10 (DDBR)	Rev 1A
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BRASWELL SOC - DISPLAY, XDP, EMMC, SD

SoC (CPU)

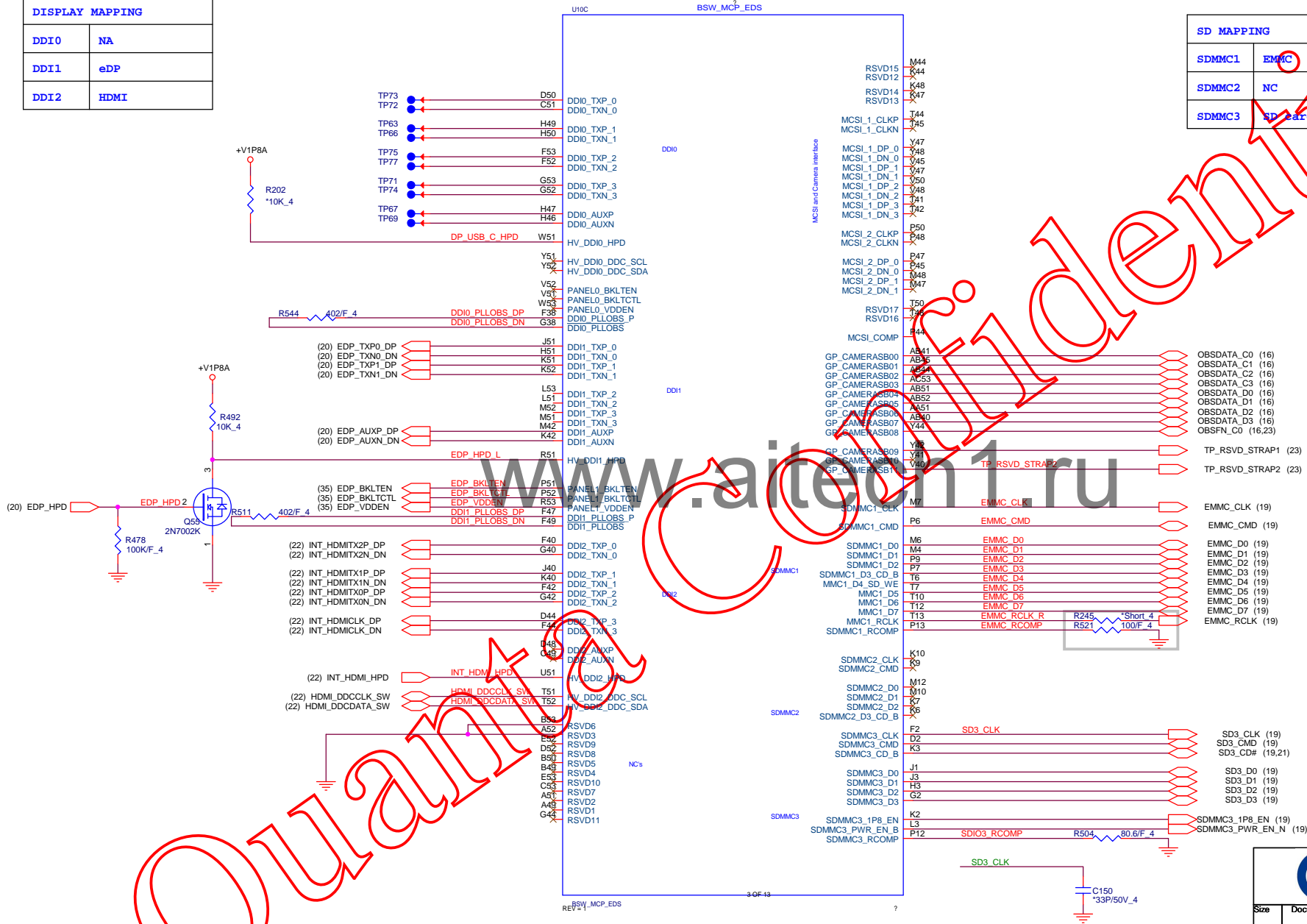
08

DISPLAY MAPPING

DDI0	NA
DDI1	eDP
DDI2	HDMI

SD MAPPING

SDMMC1	EMMC
SDMMC2	NC
SDMMC3	SP Board

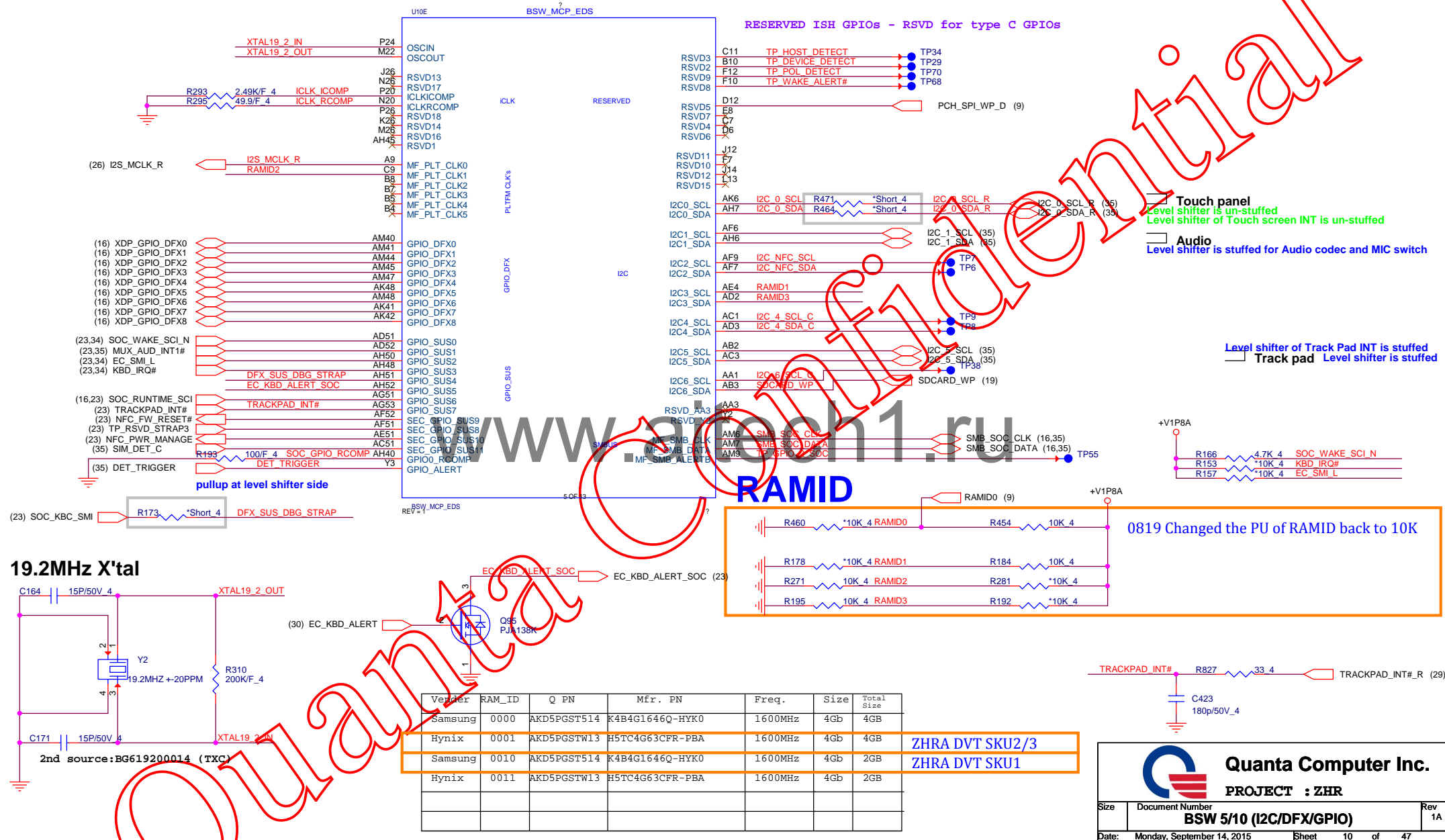


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	BSW 3/10 (DDI,SD,EMMC)	1A

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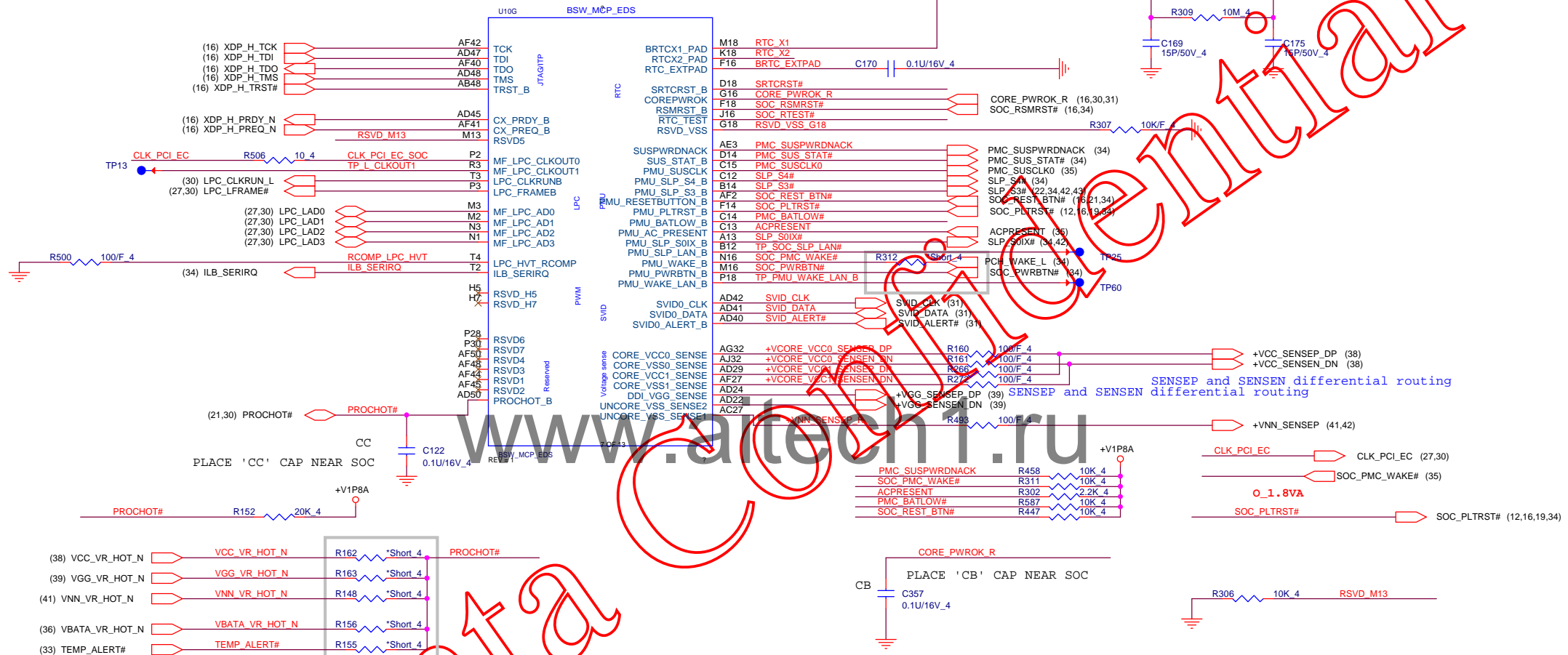
11

SOC_UART_TX R200 *0_4 SOC_UART_RX

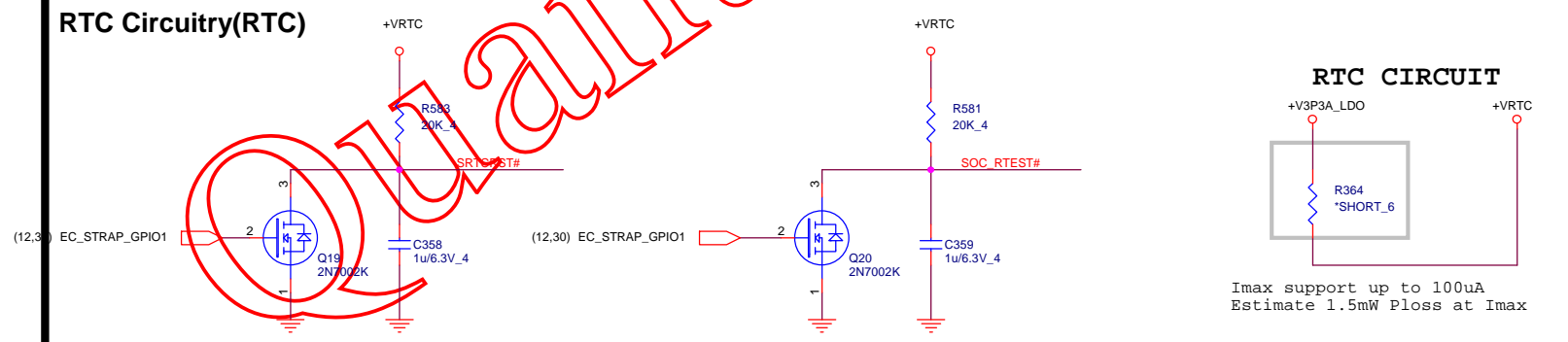
Un-Stuff for Test Only

BRASWELL - JTAG, LPC, THERMAL, PMU

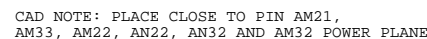
SoC (CPU)



RTC Circuitry(RTC)



Imax support up to 100uA
Estimate 1.5mW Ploss at Imax



PLACE THESE CAPS CLOSE TO AN27

+VCCCLKDDR 1P24 1P35

+VCCSFRPLLDDR 1P24 1P35

THESE CAPS
TO THE
DDQ_G_PINS

+VDDQ M0 M1 R

PLACE THESE CAPS
CLOSE TO E1 AND

+VCCPADCF3SI0 1P8 3P

PLACE T
CLOSE T

CCCEIOAZA 1P80

PLACE THESE CAPS
CLOSE TO AH4 AND

1 C309
1U/10V 4

+V1P8A R SOC

+V1P8A R SOC

PLACE THESE CAPS
CLOSE TO Y18

PLACE THESE CAPS
CLOSE TO AD33, AF33
AND AK19

+V3P3A PRIME

/CCRTCSUS 3P3

+V1P24A

1P24A R SOC

PLACE CAPS NEAR SOC

+VCCRTC 3P3

11

+V1P8A

+V1P8A R SOC

PLACE THIS CAP
CLOSE TO U16

PLACE THIS CAP
CLOSE TO G10 & H10

+VSDIO

+VCCPADCE3SI0 1P8 3P3

+V3P3A PRIME

+V1P8A

FIOAZA_1P80

+V3P3A PRIME

+VCC:ISB2 3P3

PLACE THESE CAPS
CLOSE TO THEIR PINS

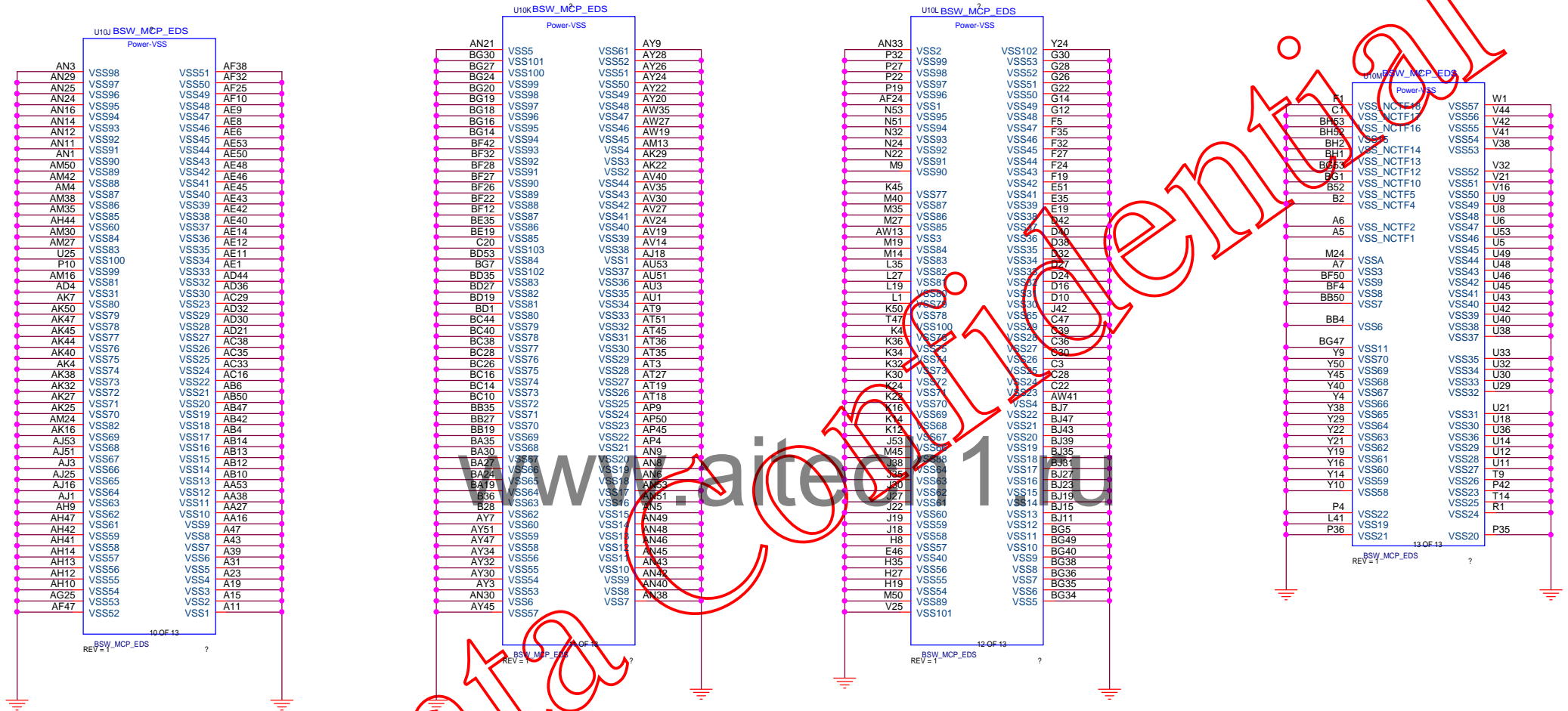


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BRASWELL - GND

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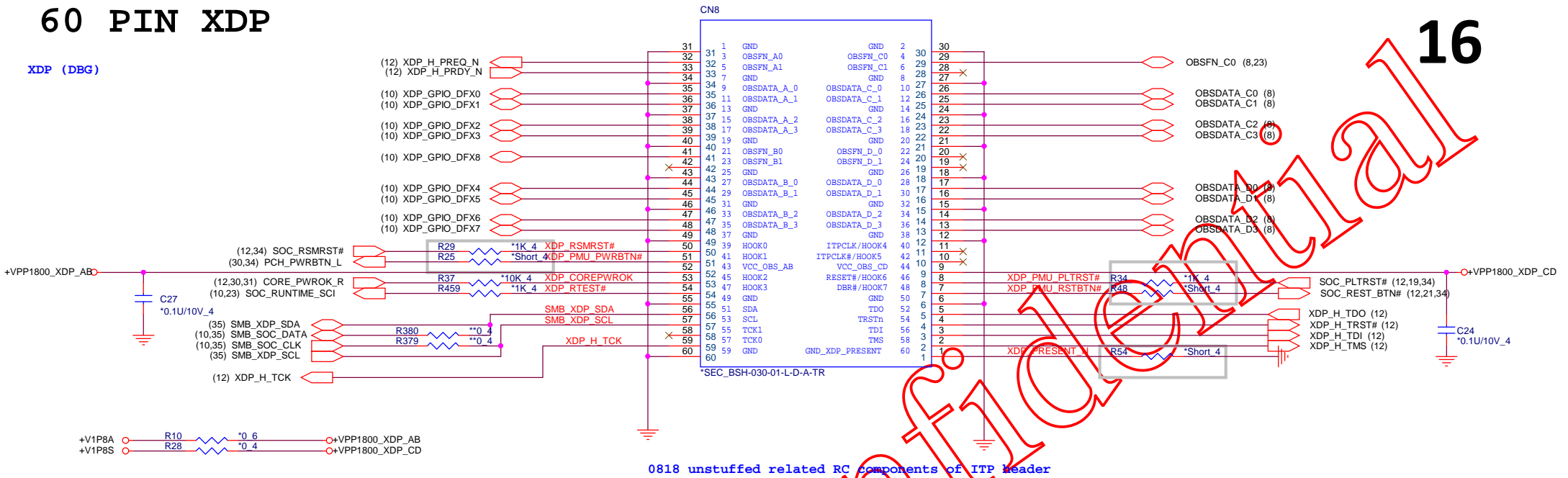
PROJECT : ZHR

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	BSW 10/10 (GND)	1A
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60 PIN XDP

XDP (DBG)

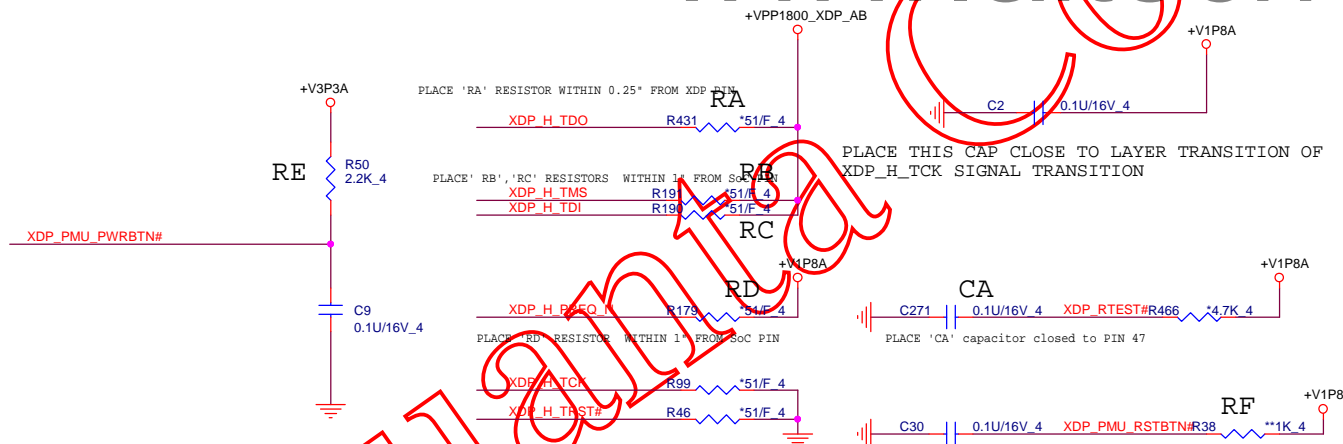
16



0818 unstuffed related RC components of ITP header

PULL-UPS AND DOWNS FOR XDP SIGNALS

APS



DDR3L MEMORY CHANNEL A

BYTE3_0-7
BYTE0_16-23

BYTE0_8-15
BYTE3_24-31

BYTE4_32-39
BYTE6_48-55

BYTE5_40-47
BYTE7_56-63

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DE-CAPS FOR MEMORY CHANNEL A

+VDDQ_M0_M1_R CAD note: Distributed around all DRAM devices (CHA)

CAD note: Place these Caps near each X16 Memory Down

Place these Caps near Memory Down CA & DQ pin

Place these Caps near Memory Down CA & DQ pin

Place these Caps near Memory Down CA & DQ pin

Place these Caps near Memory Down CA & DQ pin

Place these Caps near Memory Down CA & DQ pin

Place these Caps near Memory Down CA & DQ pin

Place these Caps near Memory Down CA & DQ pin

Place these Caps near Memory Down CA & DQ pin

Place these Caps near Memory Down CA & DQ pin

Place these Caps near Memory Down CA & DQ pin

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Place these Caps near Memory Down CA & DQ pin

Place these Caps near Memory Down CA & DQ pin

Place these Caps near Memory Down CA & DQ pin

Place these Caps near Memory Down CA & DQ pin

VTT TERMINATIONS

VOLTAGE MERGE

+VDDQ_VTT_M0_M1_R

+VDDQ_VTT_M0_M1_R

+VDDQ_VTT_M0_M1_R

+VDDQ_VTT_M0_M1_R

+VDDQ_VTT_M0_M1_R

+VDDQ_VTT_M0_M1_R

+VDDQ_VTT_M0_M1_R

+VDDQ_VTT_M0_M1_R

+VDDQ_VTT_M0_M1_R

+VDDQ_VTT_M0_M1_R

+VDDQ_VTT_M0_M1_R

+VDDQ_VTT_M0_M1_R

+VDDQ_VTT_M0_M1_R

+VDDQ_VTT_M0_M1_R

+VDDQ_VTT_M0_M1_R

+VDDQ_VTT_M0_M1_R

+VDDQ_VTT_M0_M1_R

+VDDQ_VTT_M0_M1_R

+VDDQ_VTT_M0_M1_R

+VDDQ_VTT_M0_M1_R

+VDDQ_VTT_M0_M1_R

+VDDQ_VTT_M0_M1_R

+VDDQ_VTT_M0_M1_R

+VDDQ_VTT_M0_M1_R

+VDDQ_VTT_M0_M1_R

+VDDQ_VTT

+VDDQ_VTT_M0_M1_R

+VDDQ_VTT_M0_M1_R

+VDDQ_VTT_M0_M1_R

+VDDQ_VTT_M0_M1_R

+VDDQ_VTT_M0_M1_R

+VDDQ_VTT_M0_M1_R

+VDDQ_VTT_M0_M1_R

+VDDQ_VTT_M0_M1_R

+VDDQ_VTT_M0_M1_R

+VDDQ_VTT_M0_M1_R

+VDDQ_VTT_M0_M1_R

+VDDQ_VTT_M0_M1_R

+VDDQ_VTT_M0_M1_R

+VDDQ_VTT_M0_M1_R

+VDDQ_VTT_M0_M1_R

+VDDQ_VTT_M0_M1_R

+VDDQ_VTT_M0_M1_R

+VDDQ_VTT_M0_M1_R

+VDDQ_VTT_M0_M1_R

+VDDQ_VTT_M0_M1_R

+VDDQ_VTT_M0_M1_R

+VDDQ_VTT_M0_M1_R

+VDDQ_VTT_M0_M1_R

+VDDQ_VTT_M0_M1_R

VREF_CA AND DQ CIRCUITS

+VDDQ_M0_M1_R

+VDDQ_M0_M1_R

+VDDQ_M0_M1_R

+VDDQ_M0_M1_R

+VDDQ_M0_M1_R

+VDDQ_M0_M1_R

+VDDQ_M0_M1_R

+VDDQ_M0_M1_R

+VDDQ_M0_M1_R

+VDDQ_M0_M1_R

+VDDQ_M0_M1_R

+VDDQ_M0_M1_R

+VDDQ_M0_M1_R

+VDDQ_M0_M1_R

+VDDQ_M0_M1_R

+VDDQ_M0_M1_R

+VDDQ_M0_M1_R

+VDDQ_M0_M1_R

+VDDQ_M0_M1_R

SD SLOT POWER SUPPLY

SD SLOT POWER SUPPLY

[illegible]

This is full size SD card (push-push type)

~~eMMC~~

for host interface

+V1P8S

+V3P3S

0 OHM SERIES TERMINATIONS ARE PLACEHOLDERS. VALUE MAY CHANGE

0 OHM SERIES TERMINATIONS ARE PLACEHOLDERS. VALUE MAY CHANGE

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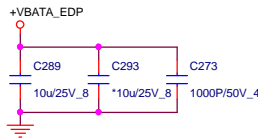
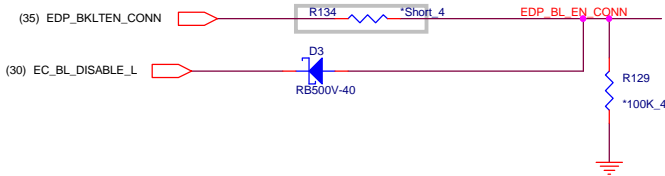
16G
Samsung-->KLMG2WEMB-B031-AKE2RF-T505-- IC FLASH (153) KLMG2WEMB-B031 (FBGA) STNBSQ
Hynix--> H26M52103FMR (0x03)--AR0ZHQRI000--PROG IC FLASH (153P) H26M52103FMR STNBSQ

32G
Samsung-->KLMBG4WECB-B031--AKE3SZ-T500--IC FLASH (153) KLMBG4WECB-B031 (FBGA) STNBSQ
Hynix--> H26M64103EMR (0x03)--AR0ZHQRI001--PROG IC FLASH (153P) H26M64103EMR STNBSQ

```

eDP PANEL CONTROL

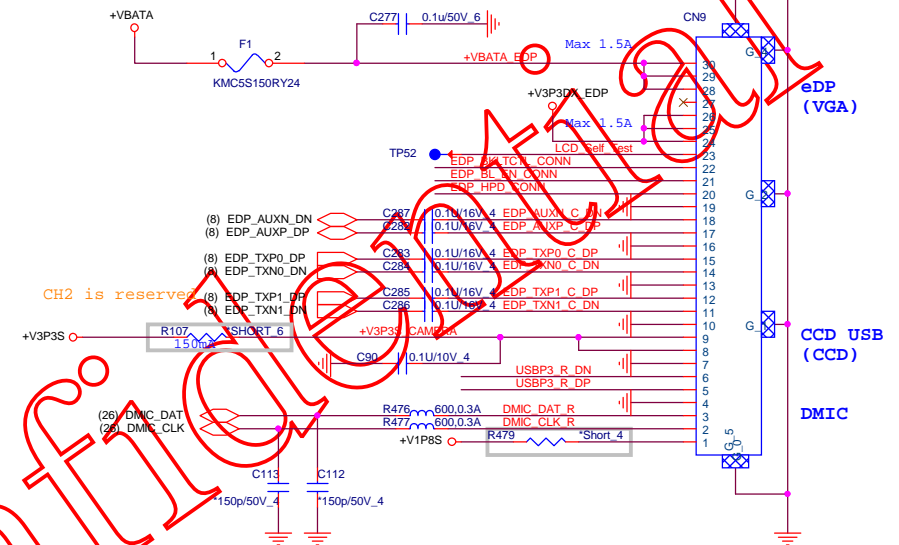
LCD(LDS)



eDP

LCD(LDS)

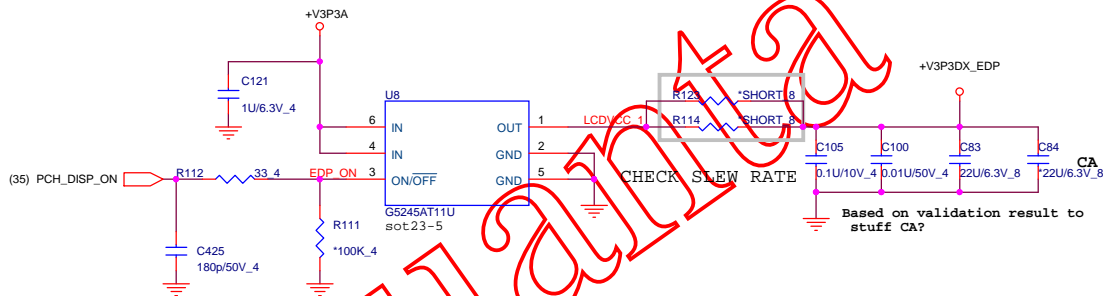
eDP CONNECTOR



20

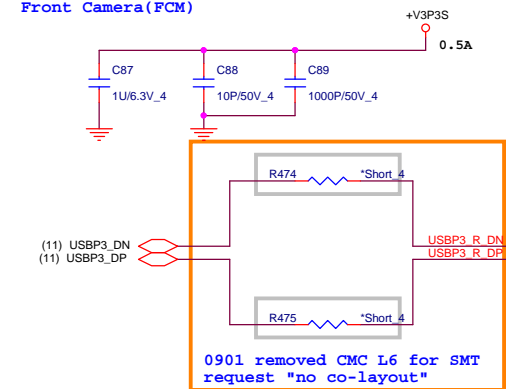
LCD(LDS)


eDP Power

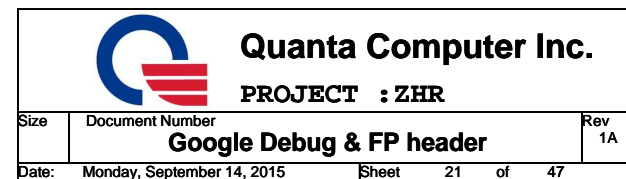


CAMERA - POWER AND USB CMC

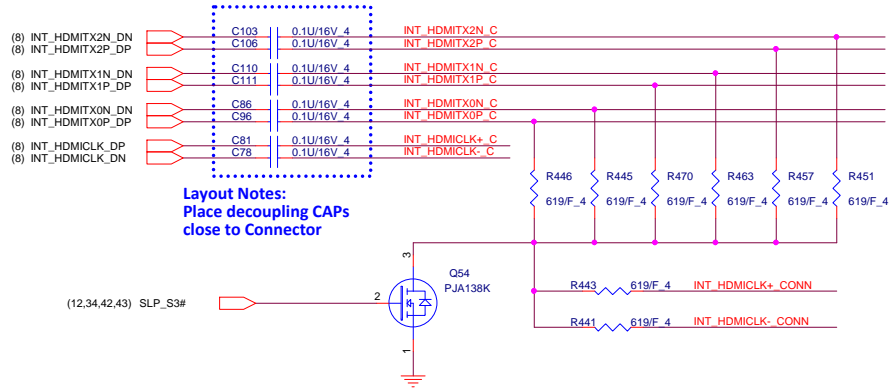
Front Camera(FCM)



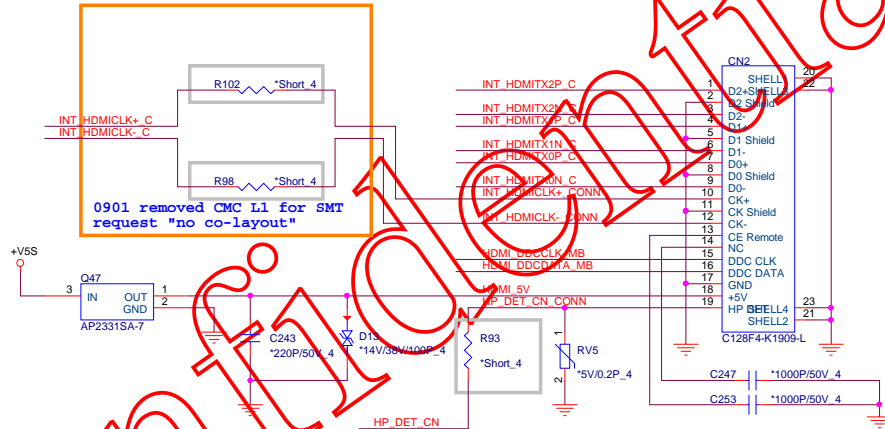
			Quanta Computer Inc.	
			PROJECT : ZHR	
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	eDP/CCD/DMIC/Touch-panel			1A
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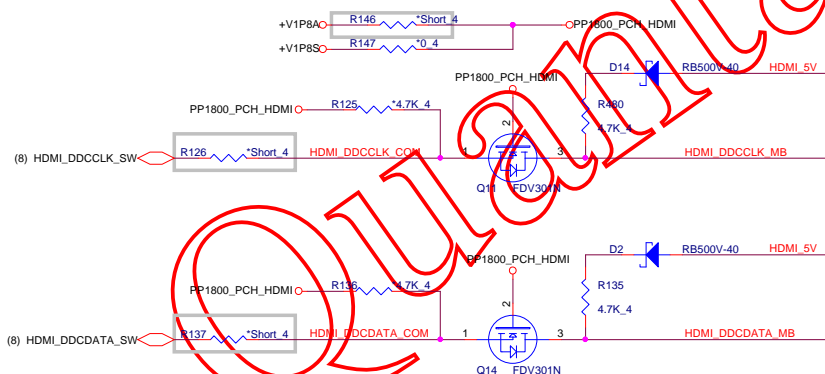
HDMI LEVEL SHIFTER



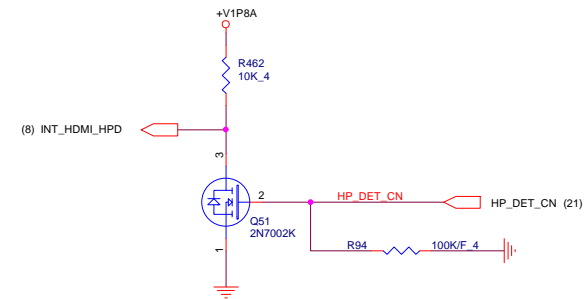
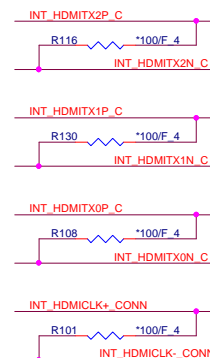
HDMI CONNECTOR



LEVEL TRANSLATOR/ EMI



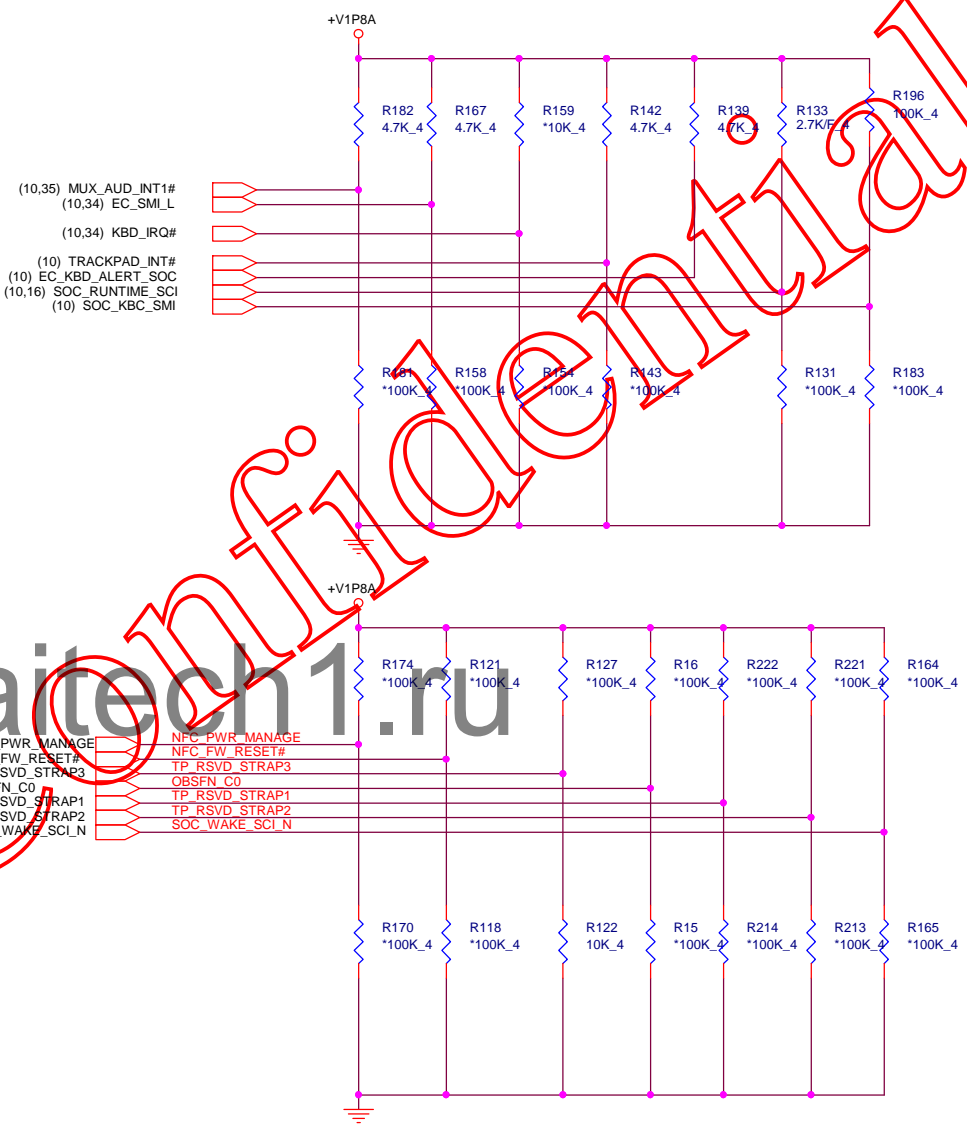
EMI



SoC (CPU)

BSW Strapping Table (based on EDS V1.0), sampled on the rising edge of PMU_RSMRST_N

Pin Name	Strap description	Configuration
GPIO_SUS0	DDI0 Detect	0 = DDI0 not detected 1 = DDI0 detected
GPIO_SUS1	DDI1 Detect	0 = DDI1 not detected 1 = DDI1 detected
GPIO_SUS2	Top Swap (A16 Override)	0 = change boot loader address 1 = Normal operation
GPIO_SUS3	DSI Display Detect (Leave floating if GPIO functionality is not used, it is not POR)	0 = DSI not detected 1 = DSI detected
GPIO_SUS4	BIOS Boot Selection	0 = No SPI 1 = SPI
GPIO_SUS5	Security Flash Descriptors	0 = Not support 1 = Normal operation
GPIO_SUS6	Halt Boot strap	1 = Normal operation (MUST be high at RSMRST# de-assert to ensure proper platform operation and use of GPIO_DFX[8:0])
GPIO_SUS7	DFX SUS DEBUG strap	0 = SUSDUG 1 = No SUSDUG
GPIO_SUS8	PLLs,ICLK,USB2,DDI ,SFR,supply select	0 = Supply is 1.25V 1 = Supply is 1.35V
GPIO_SUS9	ICLK,USB2,DDI,SFR Bypass	0 = No Bypass(Default) 1 = Bypass with 1.05V
GPIO_CAMERASB08	ICLK Xtal OSC Bypass	0 = No Bypass(Default) 1 = Bypass
GPIO_CAMERASB09	CCU SUS RO Bypass	0 = No Bypass(Default) 1 = Bypass
GPIO_CAMERASB11	RTC OSC Bypass	0 = No Bypass(Default) 1 = Bypass



WIFI/BT COMBO (NGFF E KEY)

~~24~~



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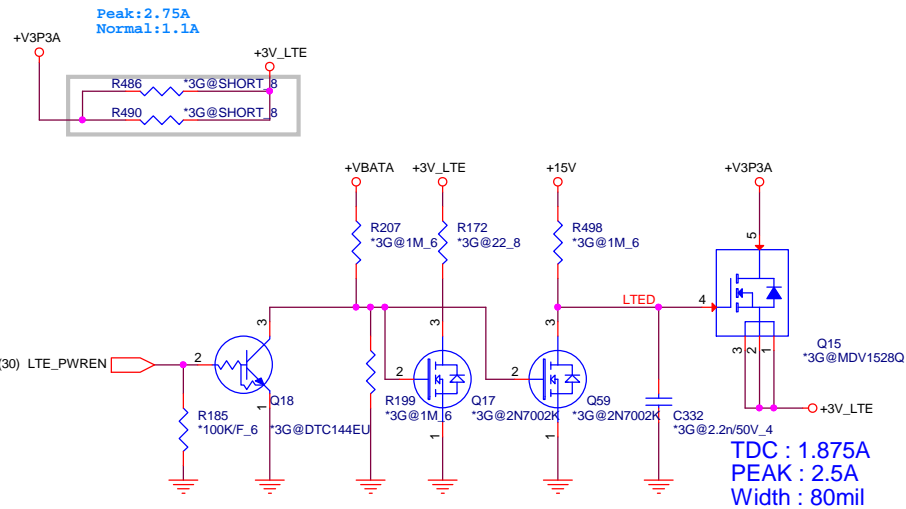
WIFI/BT(NGFF)

Rev
1A

Date: Monday, September 14, 2015

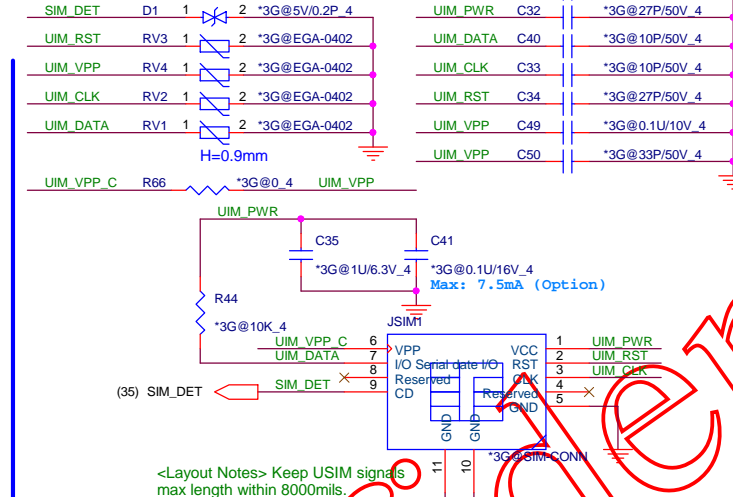
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LTE NGFF Power(LTE)



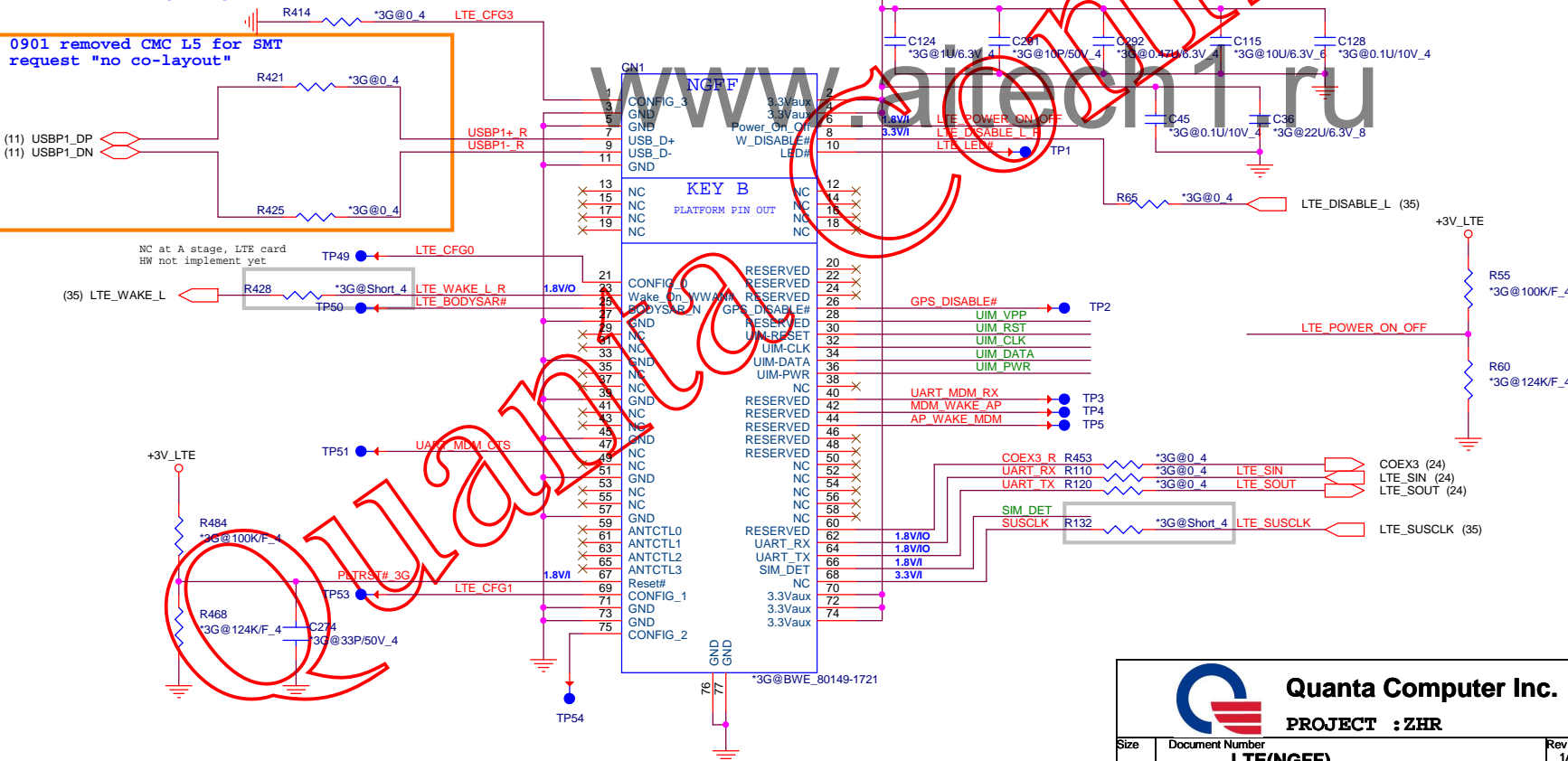
LTE

MultiMedia SIM (LTE)



25

LTE NGFF (LTE)



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Size Document Number
LTE(NGFF)

Rev 1A

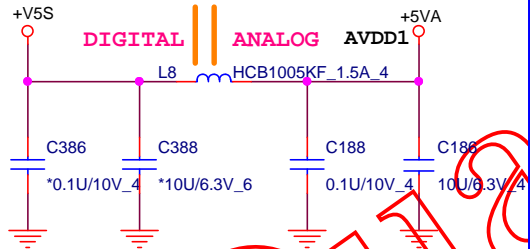
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+V1P8S

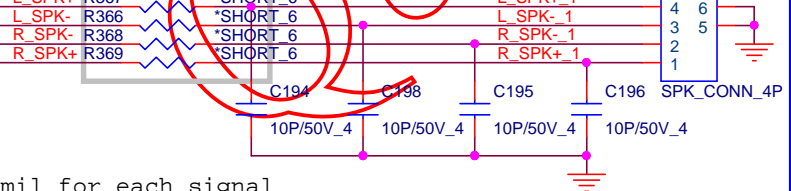
BOM Change to 0_4 due to material shortage



+V5S
DIGITAL || ANALOG AVDD



L_SPK-	R366		*SHORT_6
R_SPK-	R368		*SHORT_6



40mil for each signal

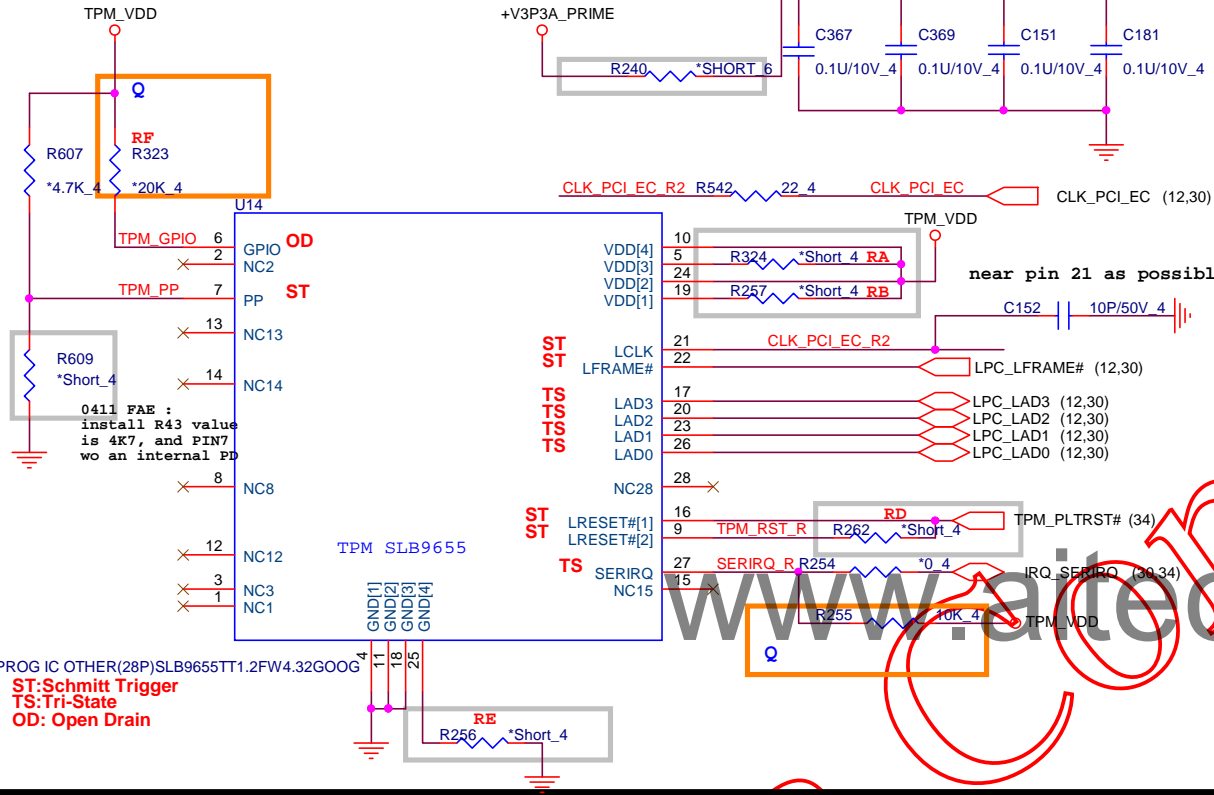
PROJECT : ZHR

Audio Codec/SPK

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TPM(TPM)

BCRD says R38 is stuffed



PROG IC OTHER(28P)SLB9655TT1.2FW4.32GOOG

ST: Schmitt Trigger

TS: Tri-State

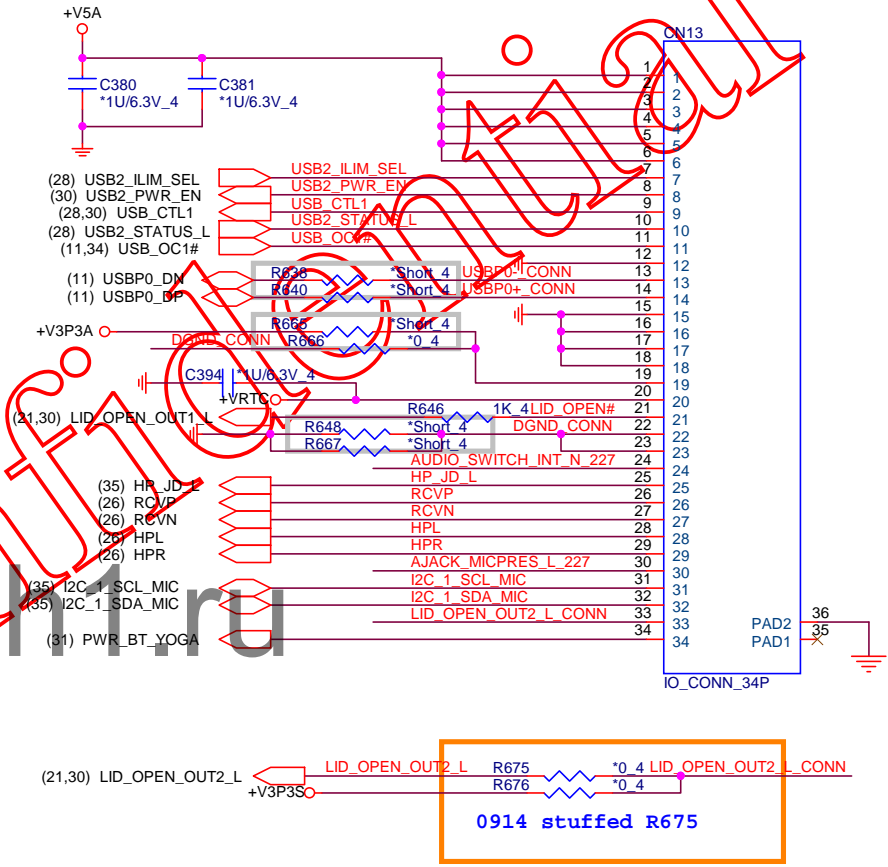
OD: Open Drain

Quanta

TPM/DAUGHTER BOARD CONNECTOR

DB(UIF)

DB CONNECTOR 27



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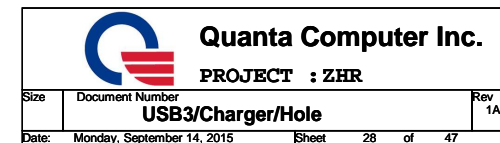
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	DB /TPM	1A
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USB3.0 (UB3) USB PWR (Charger)

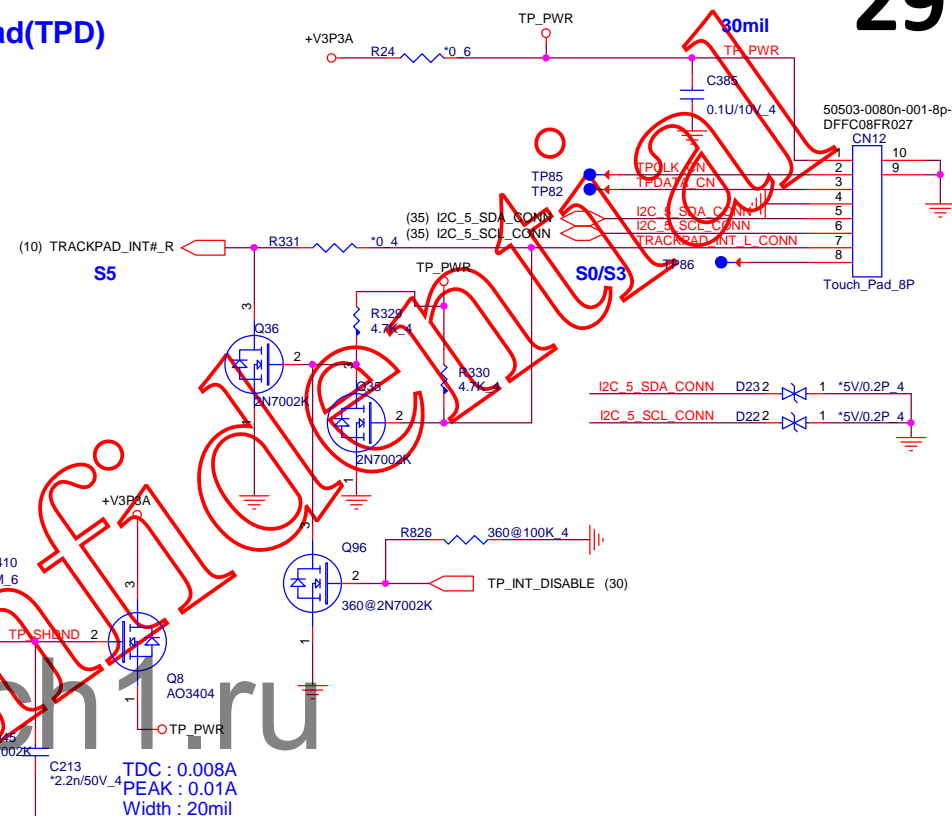
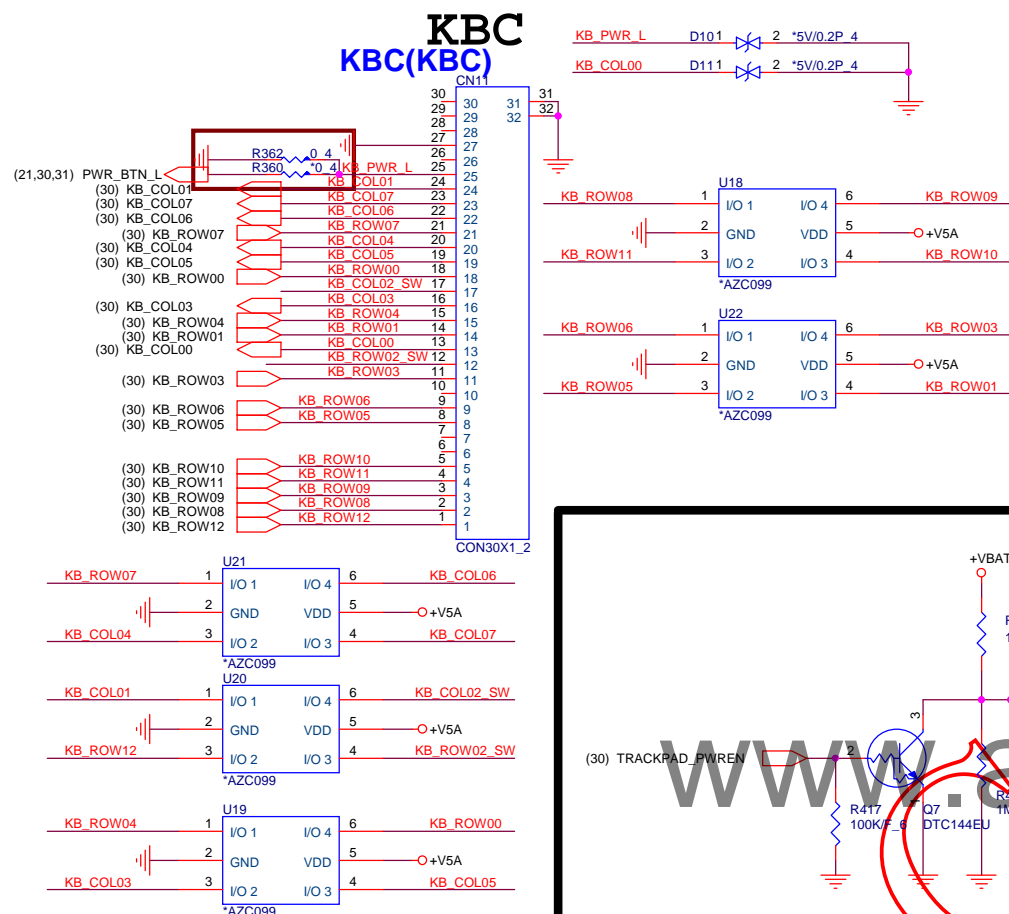
	0910 changed Hole2/Hole3 Footprints
	0911 changed Hole2 Footprints



TRACK PAD BOARD CONN

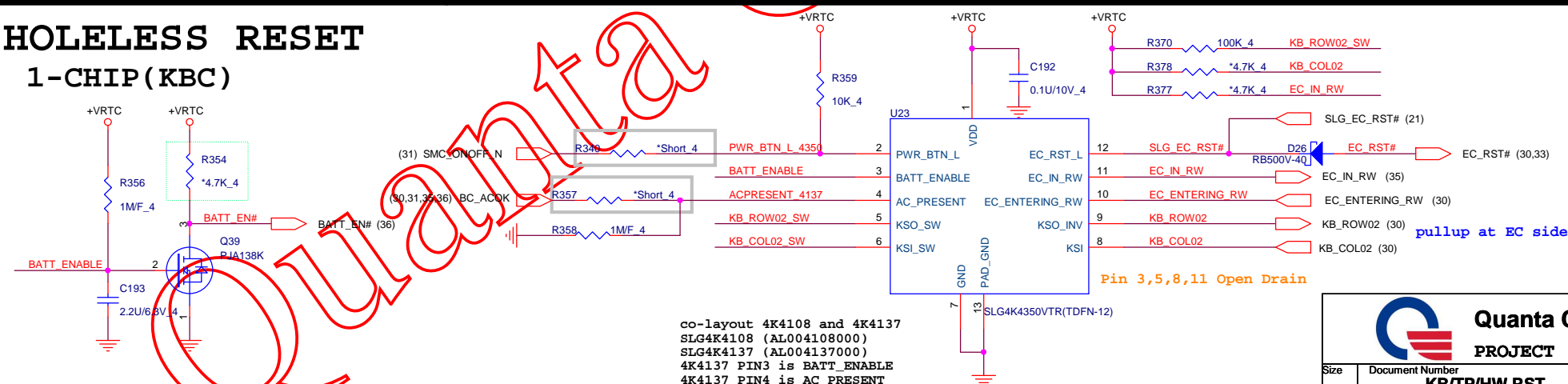
Trackpad(TPD)

KBC
KBC(KBC)



HOLELESS RESET

1-CHIP(KBC)

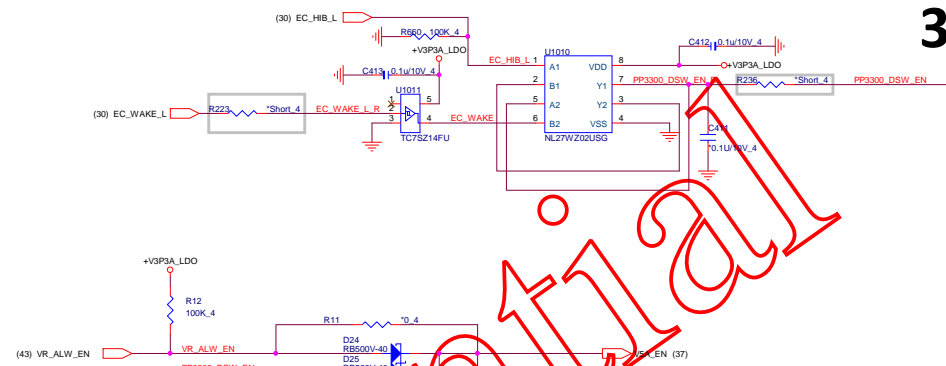
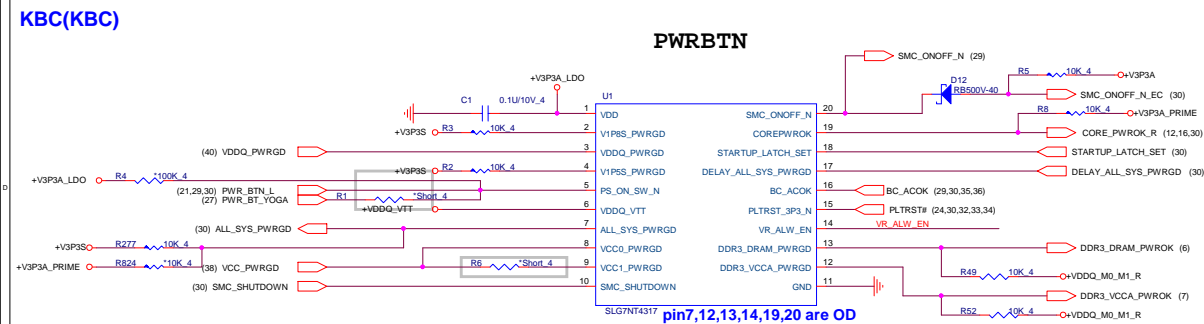


```
co-layout 4K4108 and 4K4137
SLG4K4108 (AL004108000)
SLG4K4137 (AL004137000)
4K4137 PIN3 is BATT_ENABLE
4K4137 PIN4 is AC_PRESENT
```



KBC(KBC)

PWRBTN

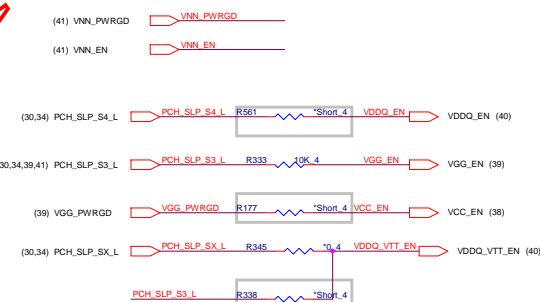
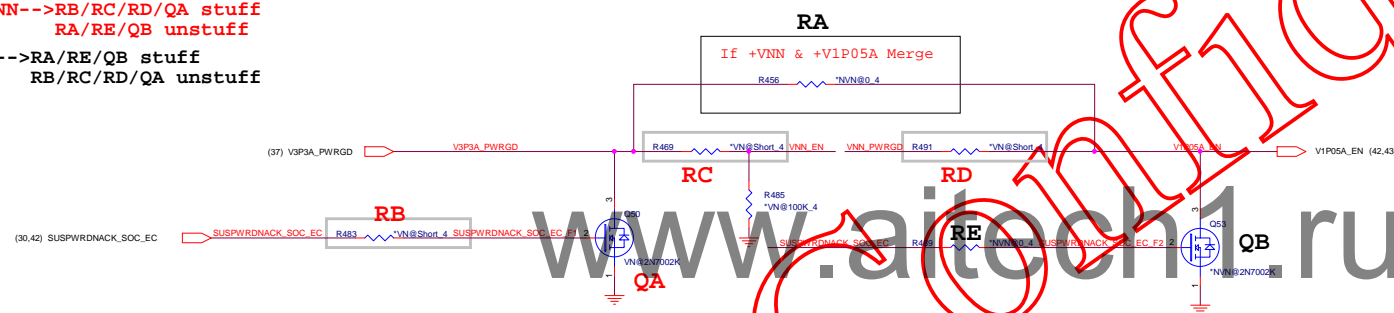


KBC(KBC)

POWER SEQUENCING

Dynamic VNN-->RB/RC/RD/QA stuff
RA/RE/QB unstuff

Fixed VNN-->RA/RE/QB stuff
RB/RC/RD/QA unstuff

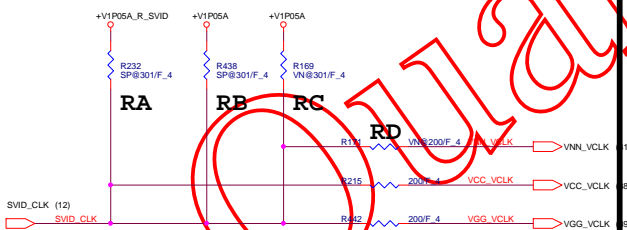


SVID(CPU)

CLK

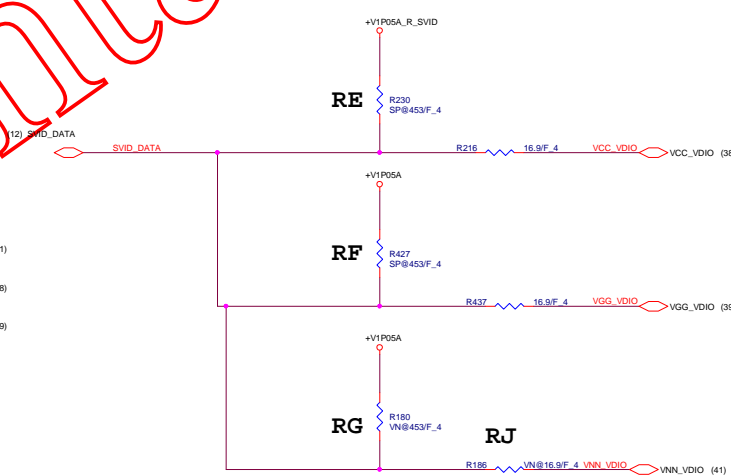
Dynamic VNN-->RA/RB/RC stuff 301 ohm
RD stuff 200 ohm

Fixed VNN-->RA/RB stuff 200 ohm,
RC/RD unstuffed



Dynamic VNN-->RE/RF/RG stuff 453 ohm
RJ stuff 16.9 ohm

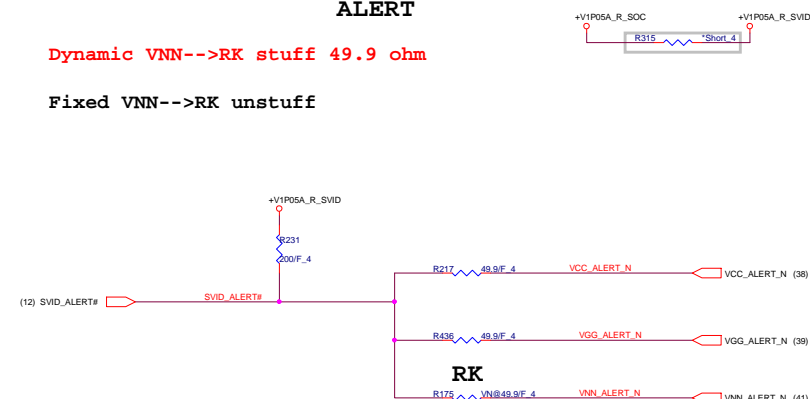
Fixed VNN-->RE/RF stuff 301 ohm,
RG/RJ unstuffed

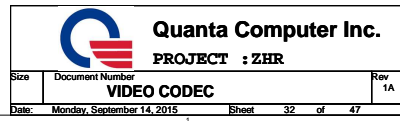


ALERT

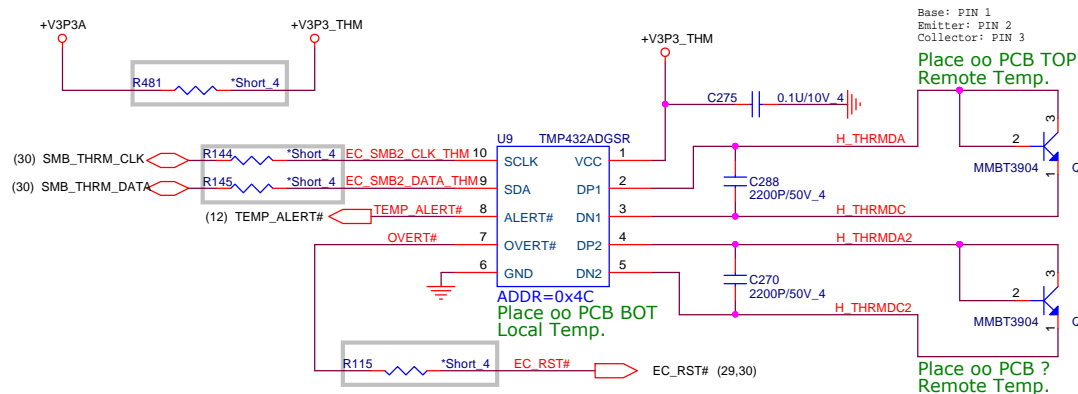
Dynamic VNN-->RK stuff 49.9 ohm

Fixed VNN-->RK unstuff



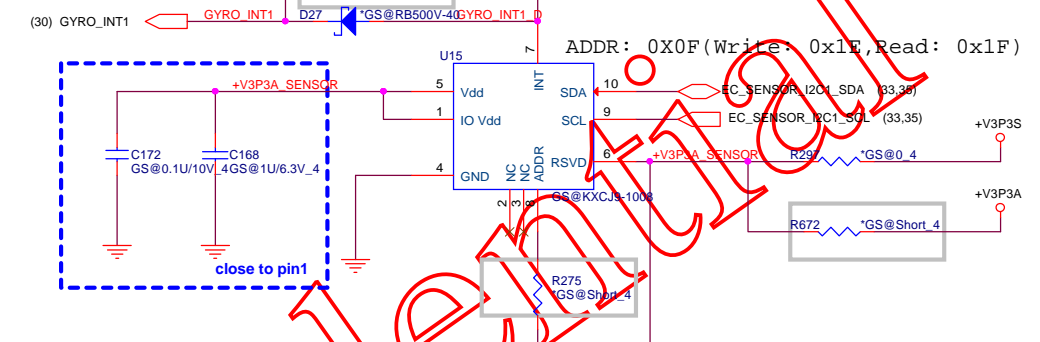


THERMAL SENSOR SENSORS/Touch screen Board/LED Board



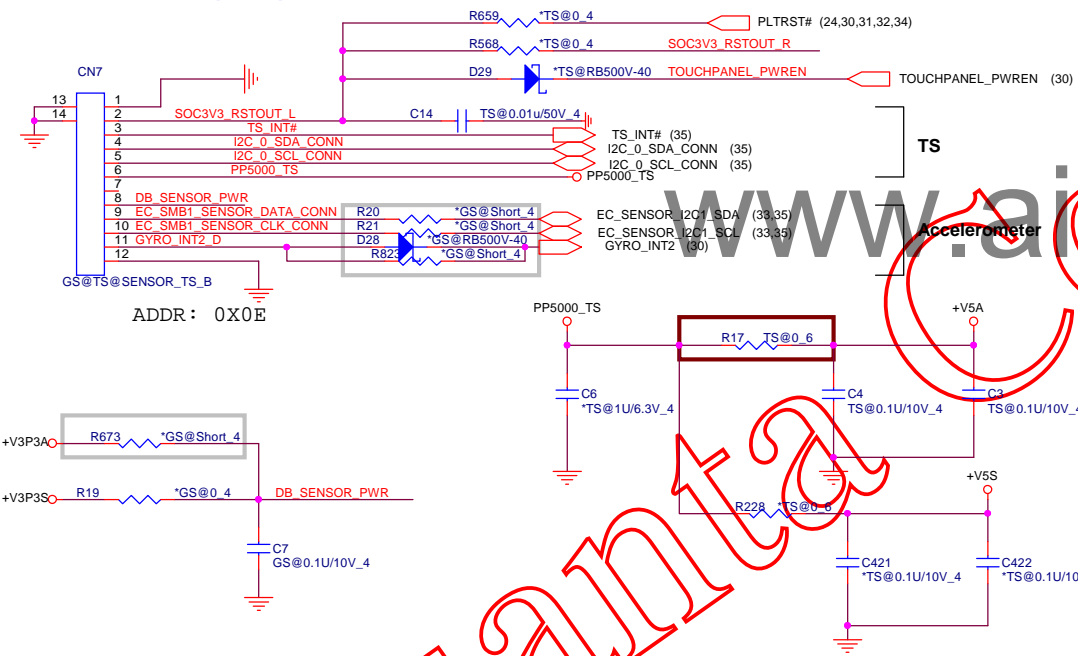
ACCELEROMETER

G-Sensor (ACS)

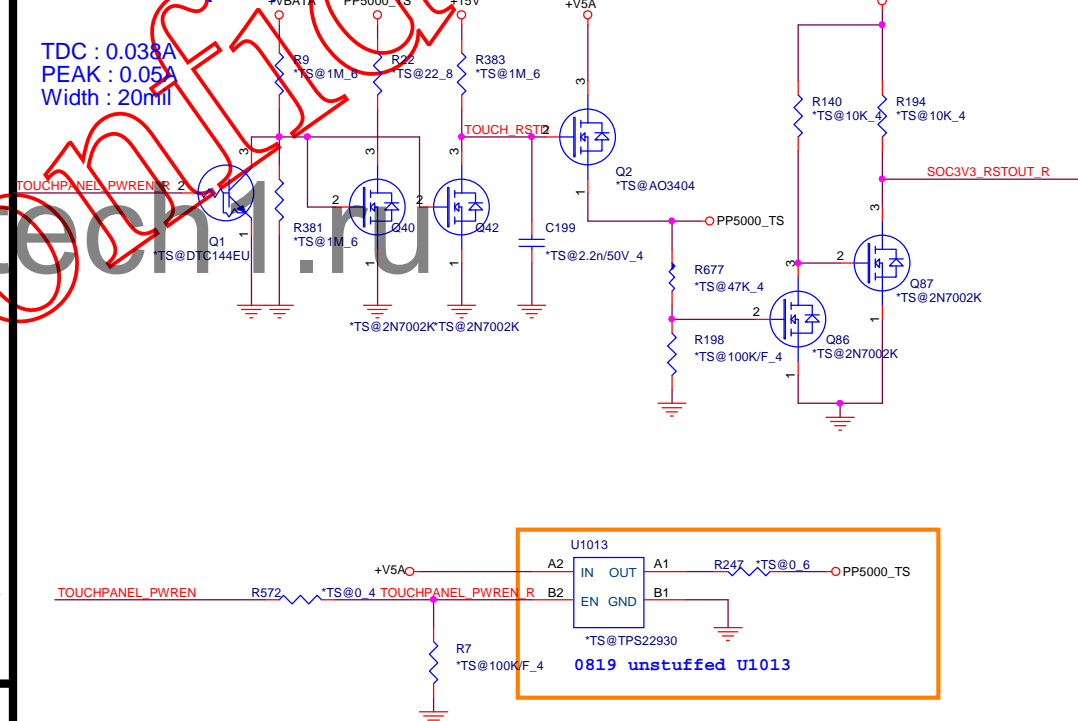


33

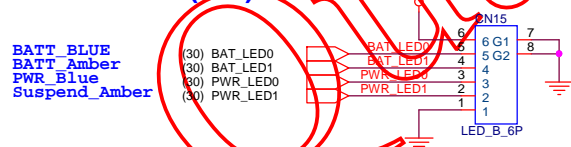
Touch screen(TSN)



Touch screen(TSN)

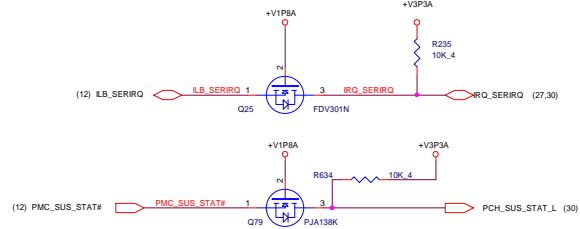


LED board(UIF)

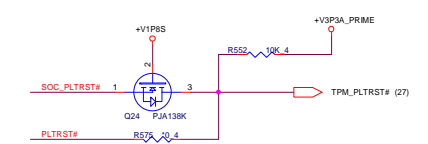
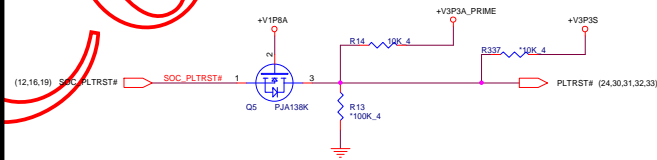
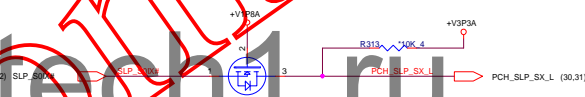
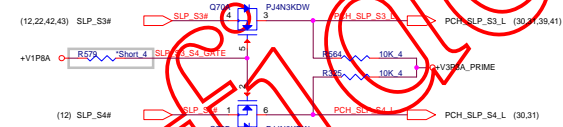
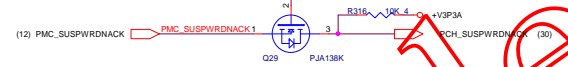
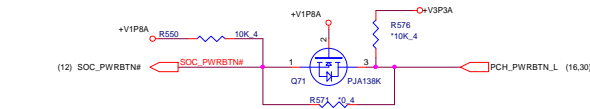


SoC(CPU)

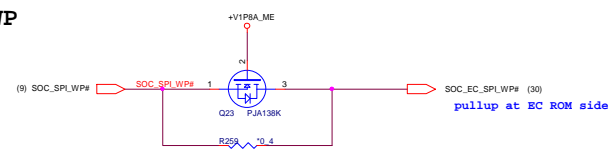
PWRON SEQUENCE



PWRON SEQUENCE

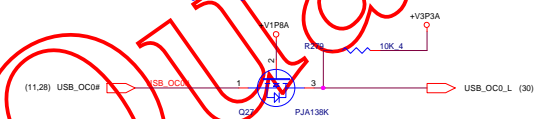


ROM WP

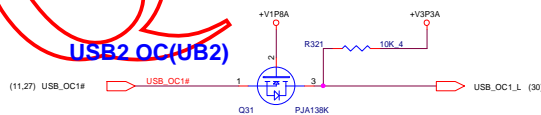


USB OC

USB3 OC(UB3)



USB2 OC(UB2)



NOTE:USE 4 BIT LEVEL TRANSLATORS

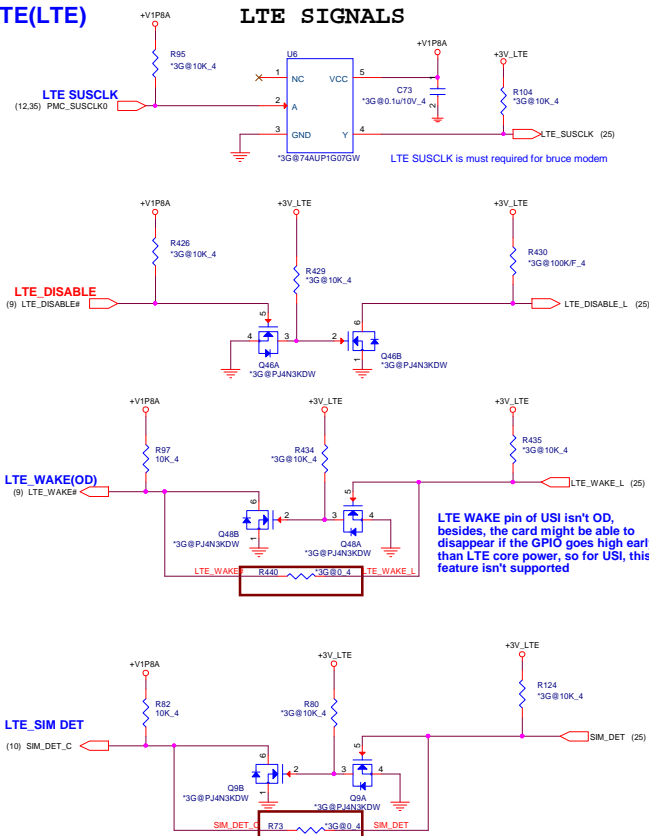
LEVEL TRANSLATOR 2

TRACK PAD I2C_5 SIGNALS

35

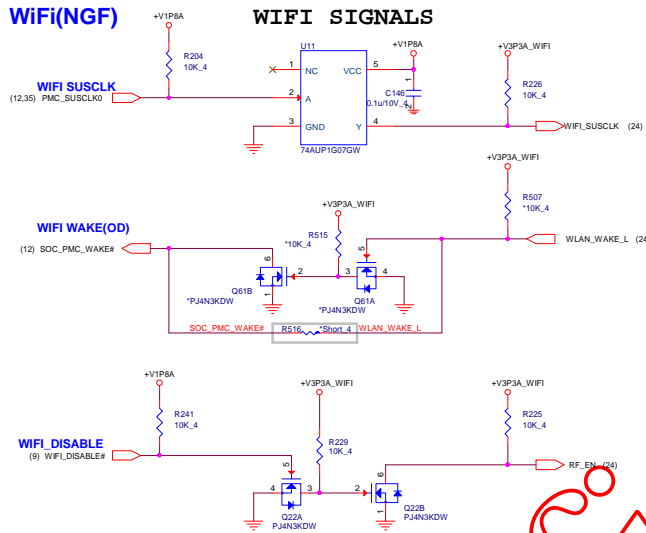
LTE(LTE)

LTE SIGNALS

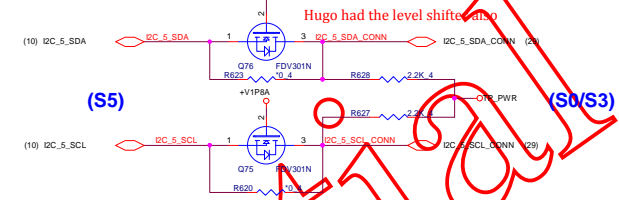


WiFi(NGF)

WIFI SIGNALS

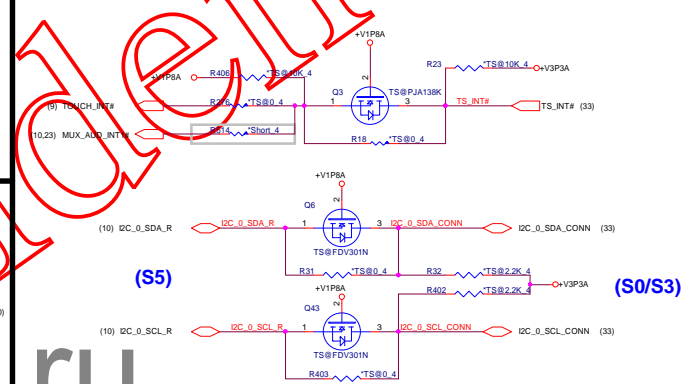


Trackpad(TPD)

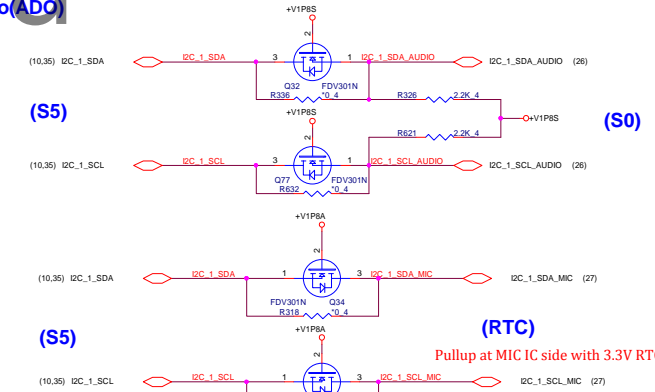


Touch Screen(TSN)

TOUCH SCREEN I2C_0 SIGNALS

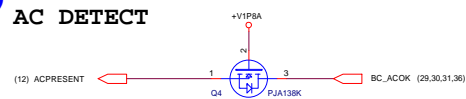


Audio(ADO)



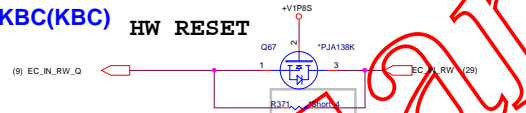
KBC(KBC)

AC DETECT

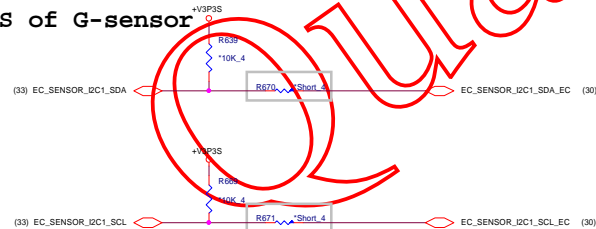


KBC(KBC)

HW RESET

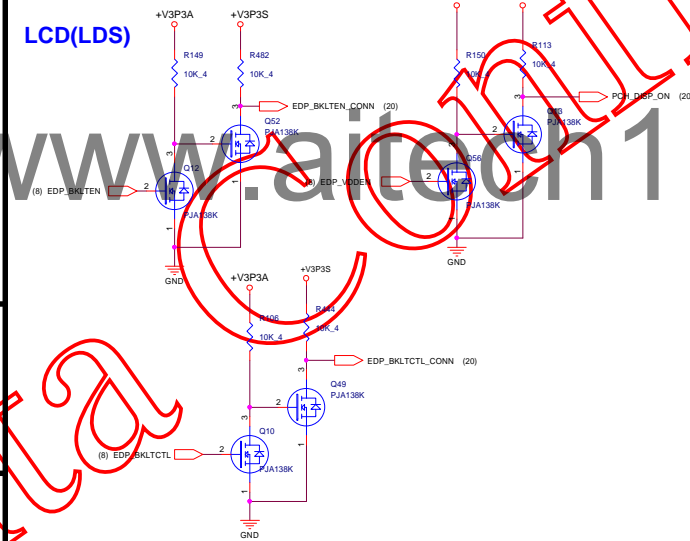


LS of G-sensor

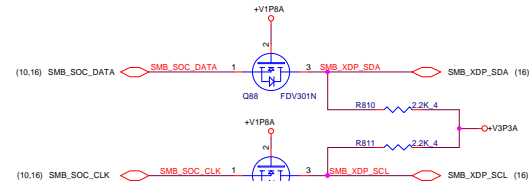


eDP CONTROL PIN

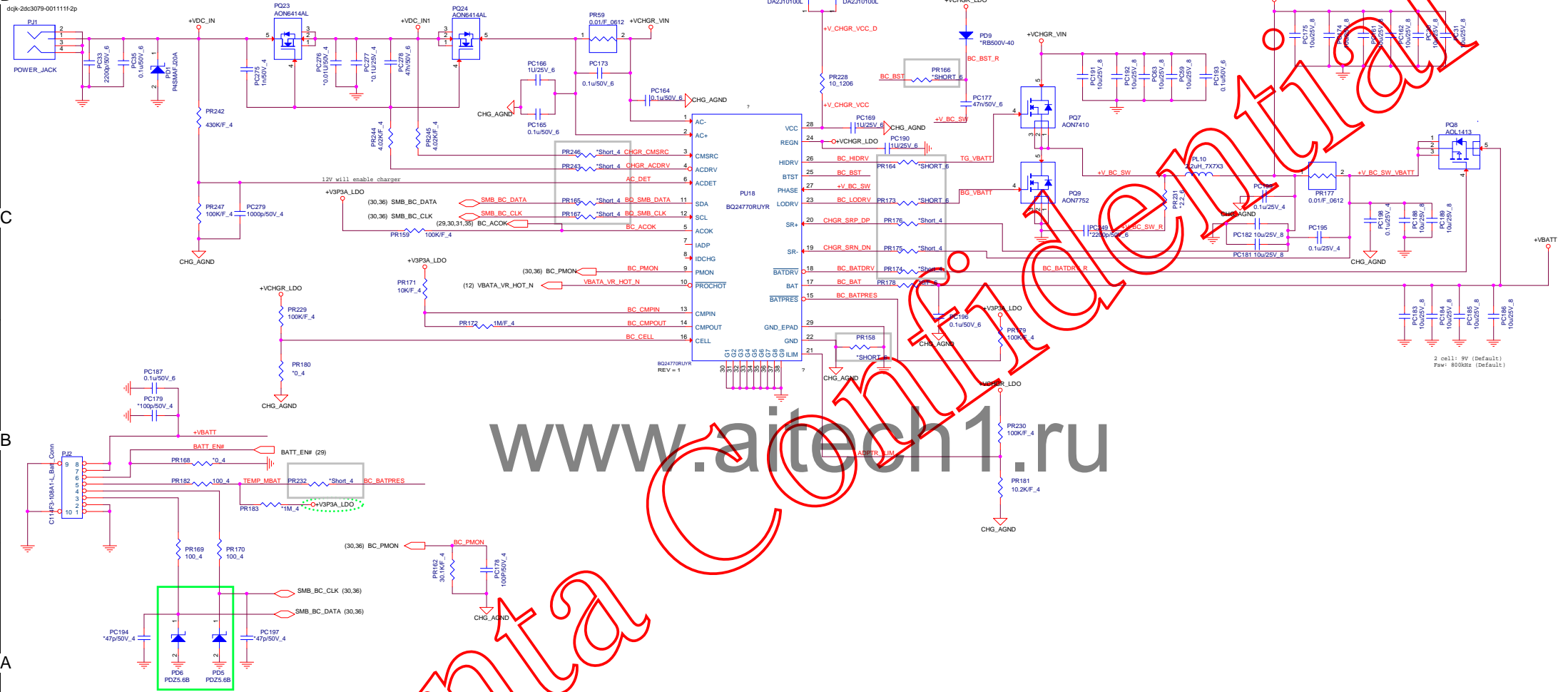
LCD(LDS)



LS of XDP SMBUS

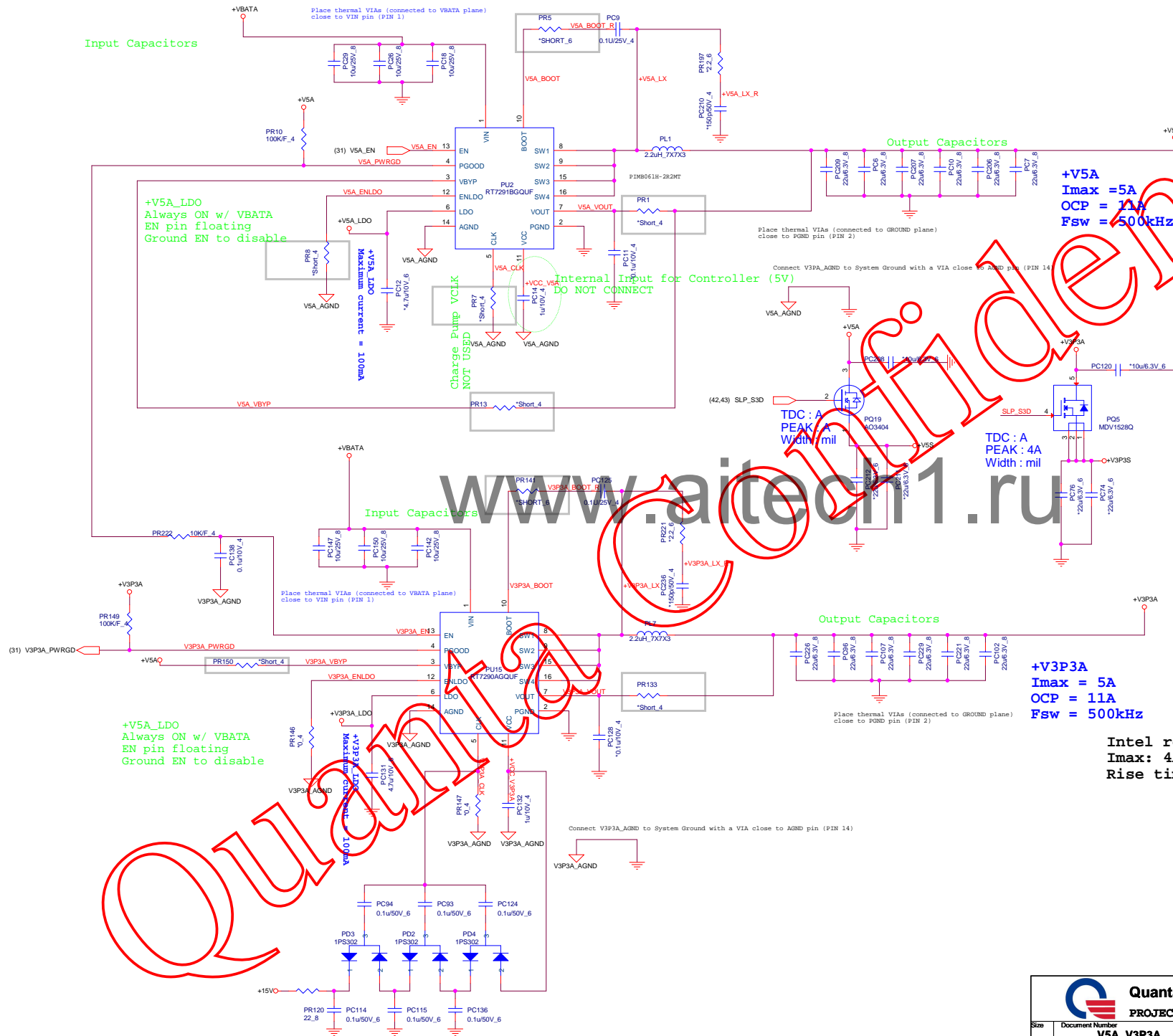


dck-2dc3079-0011111-2p



VR PAGE: +V5A & +V3P3A

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VR PAGE: VCC_CPU

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SET1:
Comp. Ramp factor = 267%
DVID width = 72us
DVID threshold = 15mV

SET2:
Icc,max = 7A
QR trigger = disable
QR width / Ton = 111%

SET3:
ZCD threshold = 75mV
Anti-overshoot = enabled
Fsw > 500kHz
VR Address = 0

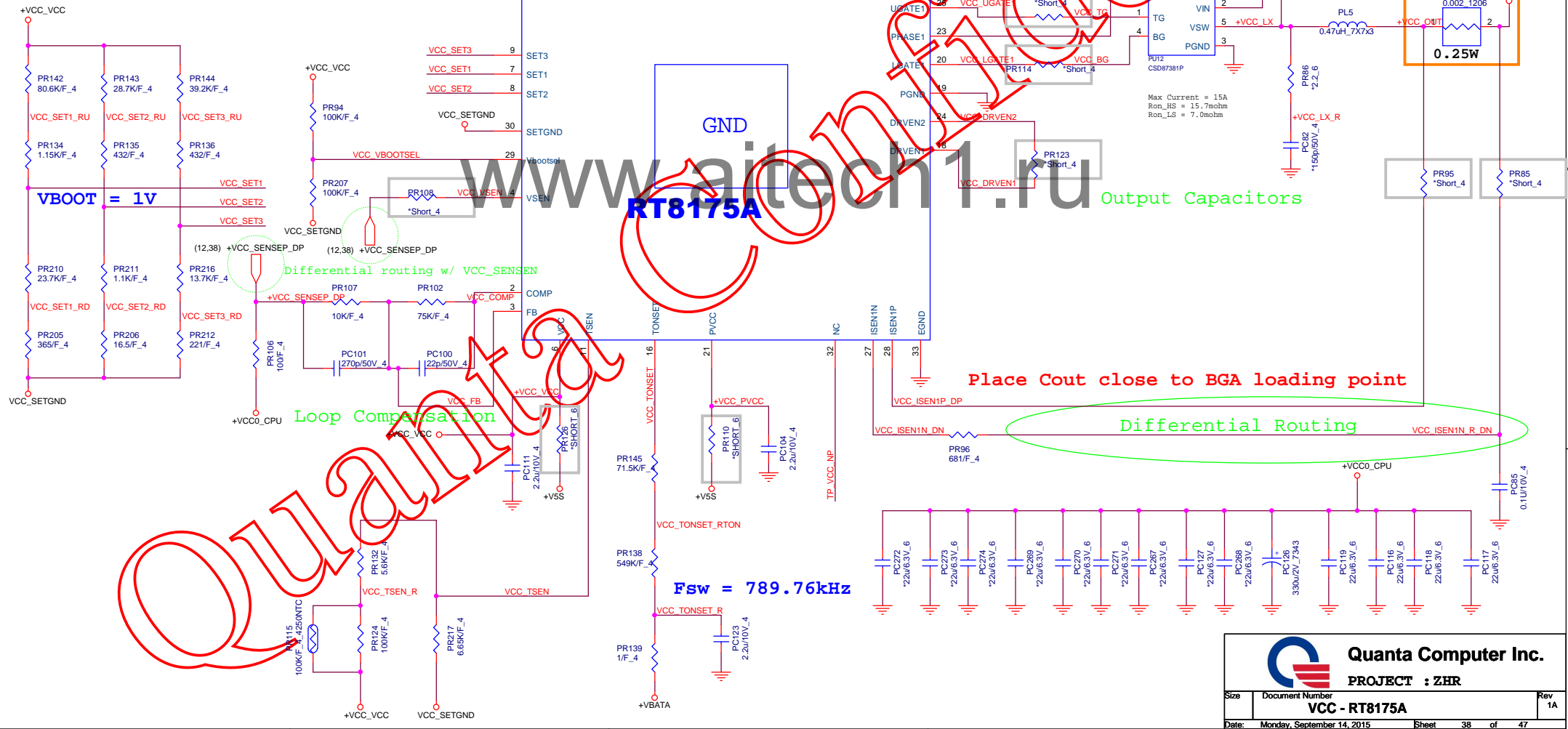
REQ = 19.43kohm

Place Cin close to FET VIN pin
(1uF closer to VIN)

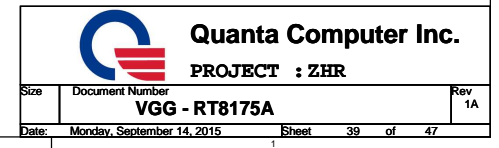
SVID Interface

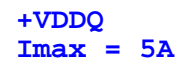
Input Capacitors

+VCC_CPU
Imax = 7 A
OCP = 8.96A (128%)
Load-line = 0ohm




```
SET3:
ZCD threshold = 75mV
Anti-overshoot = enabled
Fsw > 500kHz
VR Address = 5
```





Date: Monday, September 14, 2015 Sheet 40 of 47

SET1:
Comp. Ramp factor = 267%
DIVID width = 72us
DIVID threshold = 15mV

SET2:
Icc,max = 4.0 A
QR trigger = disable
QR width / Ton = 111%

SET3:
ZCD threshold = .75mV
Anti-overshoot = enabled
Fsw > 500kHz
VR Address = 01b

0W02.2 - Resistor value change :
R3A100 => 33.2K
R3A200 => 4.7K
R3A300 => 976

REQ = 38.86 kohm

Place Cin close to FET VIN pin
(1uF closer to VIN)

SVID Interface

Input Capacitors

+VNN : 0.78 - 1.2V
I_{max} = 3.5 A
OCF = 5.0 A (128%)
Load-line = 0.5hm

0W02.2 - changed to +VNN_VDD

0W02.2 - Resistor value change :
R3A1200 => 1.15K
R3A1300 => 481
R3A1400 => 392
R3A1500 => 221
R3A1600 => 13.7 K

Design Note : ->
optimized for standby current

VNN OFFSET BACKUP CIRCUIT

Loop Compensation

VNN OFFSET CIRCUIT

Fsw = 803.43kHz

Differential Routing

Output Capacitors

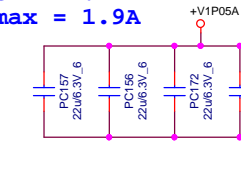
0W02.2 output caps are changed to 5X47 uF

Place Cout close to BGA loading point

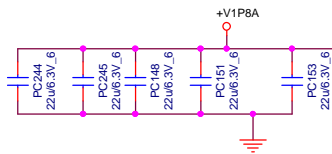
To SOC VNN Package Sensing
(+VNN merge with +V1P05A)

V1P05A Output Sensing

V1P05A (Buck)
Fsw = 1.2MHz
Imax = 1.9A



V1P8A (Buck)
Fsw = 1.2MHz
Imax = 1.8A



MOIC EN_1P05A PR223 *Short 4
MOIC SUSPWRDNACK PR167 *Short 4
MOIC SLP_S3D PR151 *Short 4
MOIC SLP_S3B PR151 *Short 4

+V1P05A_EN (31,43)
SUSPWRDNACK_SOC_EC (30,31)
SLP_S0IX# (12,34)
SLP_S3# (12,22,34,43)

Intel requirement
Imax: 1A
Rise time: 1ms

TDC: A
PEAK: 1A
Width: mil

V3P3A_PRIME
Load Switch
Imax = 200mA

V1P8A Output Sensing

V1P8A_PRIME
Load Switch
- NOT USED -

V1P24A
LDO
Imax = 550mA

V1P15A
LDO
Imax = 700mA

V1P5S
LDO
Imax = 17mA

MOIC_O_1P05A

+V MOIC_VCC

MOIC_SLP_1P05A
MOIC_SUSPWRDNACK
MOIC_SLP_S3D
MOIC_SLP_S3B
MOIC_RSMRST

+V3P3A_PRIME

MOIC_O_1P8

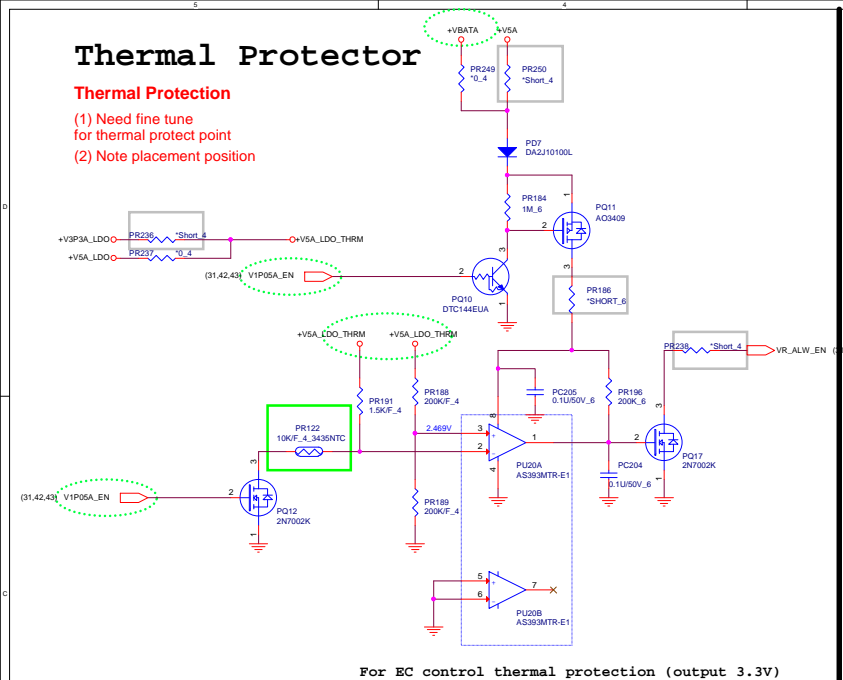
+V MOIC_LX_1P05A
+V MOIC_LX_1P8

+V1P05A_LX_R
+V1P8A_LX_R

+V1P8A

+V1P8S

- (1) Need fine tune for thermal protect point
- (2) Note placement position



For EC control thermal protection (output 3.3V)

(12,22,34,42,43) SLP_S3W

PR195 100KUF, 5

PQ18 DTC144EU

PR192 1MVA

PQ14 2N7002K

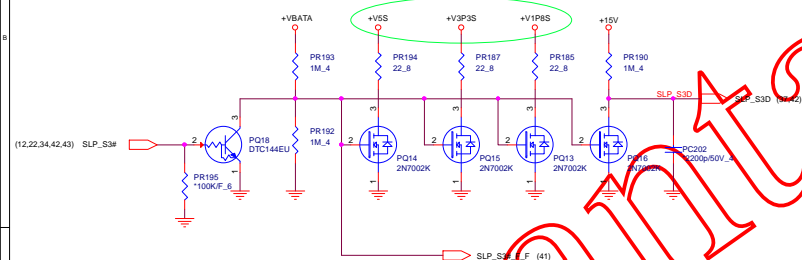
PQ15 2N7002K

PQ13 2N7002K

PQ16 2N7002K

PCC002 5V

SLP_S3W (41)



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Video codec(VDC)

DESIGN NOTE:
Delay 15 ns max
500 max=400 mA

PCB FP required

0818 unstuffed related RC components of Kepler

0818 unstuffed related RC components of Kepler

www.aitech1.ru

0818 unstuffed related RC components of current sensor

0819 Deleted all current sensor INA219

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Quanta

Confidential

0818 unstuffed related RC components of current sensor

0819 Deleted all current sensor INA219

Confidential

[illegible]